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HIGH-THERMAL-CONDUCTIVITY AIN PACKAGES FOR HIGH-TEMPERATURE ELECTRONICS

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A novel metallization for aluminum nitride substrates to package silicon carbide integrated circuits for use at temperatures of 600°C and above was investigated. Chemical equilibrium calculations were used to determine the chemical compatibility of several refractory and transition metal disilicides with AlN and SiC. Tungsten disilicide, niobium disilicide, and titanium disilicide were selected for diffusion couple and thin film deposition studies. AlN-WSi_2-SiC, AlN-$NbSi_2$-SiC, and AlN-$TiSi_2$-SiC diffusion couples were formed at 1000°C and 1200°C. WSi_2, $NbSi_2$, and $TiSi_2$ thin films were deposited by RF sputtering on AlN substrates and heat treated at 900°C, 1000°C, and 1200°C in an argon atmosphere, while WSi_2 thin film was deposited on a single-crystal SiC wafer and heat treated at 900°C. Sheet resistivities were measured, and interfaces were characterized by scanning and transmission electron microscopy imaging, electron diffraction, and energy-dispersive x-ray microanalysis spectroscopy. The results show that metal silicides appear to be promising as metallization for aluminum nitride for use at 600°C and above.

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Aluminum nitride, Ceramic package, High-temperature electronics, Interconnects, Metallization, Silicon carbide device

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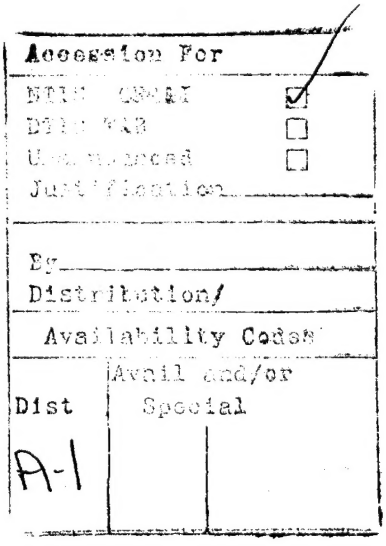

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1. INTRODUCTION

There is a growing need for electronic devices, circuits, and systems that can operate at high temperatures. The automotive industry has many applications, such as in under-hood areas, where temperatures approach 200°C, and in exhaust sensors and controllers, where peak temperatures can reach 650°C (Waite, 1981). For avionics engine monitoring and control, such as in the Air Force Mostly Electric Aircraft (MEA), electronic devices are required that are capable of reliable operation at temperatures as high as 400°C (Palkuti et al., 1979; Reinhardt et al., 1995). To ensure reliability for safe aircraft operation, device performance requirements can easily be extended to the 500-600°C temperature range (Nieberding and Powell, 1982). Space applications can expose spacecraft and their electronics to temperatures as high as 400°C (Jurgens, 1982). The nuclear power, heavy industrial manufacturing, and petroleum industries expose sensors and control electronics to temperatures above 400°C (Palmer and Heckman, 1978; Traeger and Lysne, 1988).

Regardless of application, the keys to successful high-temperature electronics are the availability of stable high-temperature electronic components (integrated circuits, resistors, capacitors, etc.) and the packaging of these components using the proper materials. The development of silicon carbide integrated circuit (SiC IC) devices for use at temperatures up to 600°C has been well underway for these applications. But without parallel developments in packaging technology, the advances in SiC ICs will not much matter. Unless there is a way for the SiC ICs to communicate with the outside world, they will not be useful. Package selection and development are critical factors in meeting several key requirements: thermal and electrical performance, cost, and form factor. Even though aluminum nitride and other ceramic packages are available for room-temperature electronics, none of them is suitable to package SiC ICs for high-temperature and/or high-power applications. Off-the-shelf packages lack thermal conductivity, thermal expansion coefficient (CTE) match to the silicon carbide, and stable metallization at high temperatures. Therefore, there is a significant need for a package development for SiC ICs suitable for continuous operation at temperatures of 600°C and above.

In this Phase I STTR project, QUEST Integrated, Inc., and the University of Washington have conducted research to develop aluminum nitride packaging for SiC ICs for high-temperature (600°C and above) operation. This final report documents the Phase I effort.

2. HIGH-TEMPERATURE PACKAGING DESIGN ISSUES

A package and an IC are thermally and mechanically coupled as shown in Figure 1. The IC die must be attached to the package and the wire bonding to leads. The package must provide an electrical connection between the microworld of the SiC IC chip and the macroworld of the system as well as protection for the device, and it must also allow for dissipation of the heat generated by the device (the SiC IC). Therefore, a system approach to package development is required; this system approach and the research needs should be considered together as a unit.

Figure 2 illustrates the functions of a package. Material properties can significantly impact how well the package can meet its requirements. The design of high-temperature packages is primarily influenced by the available materials. High-temperature packaging design issues include the following:

- ***Thermal conductivity***: The Air Force MEA program involves power devices such as motor controls that produce large amounts of heat, up to 100 W/cm^2 (Mahefkey, 1994). These devices require a high-thermal-conductivity path for removing heat to maintain the die at a safe operating temperature. If the die temperature exceeds the safe operating temperature, the device will fail prematurely. Therefore, system thermal resistance must be minimized. Substrate, metallization, and die attach thermal conductivity must be maximized. The fact that the thermal conductivity of packaging materials decreases with increasing temperature must be considered.

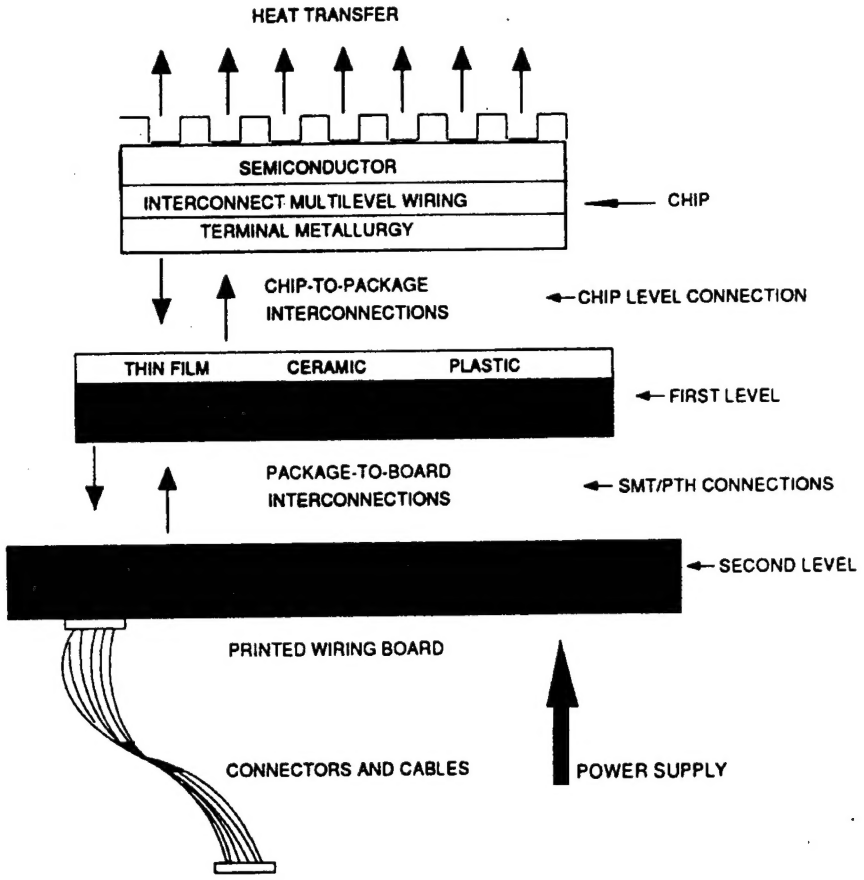

Figure 1. IC chip and packaging hierarchy.

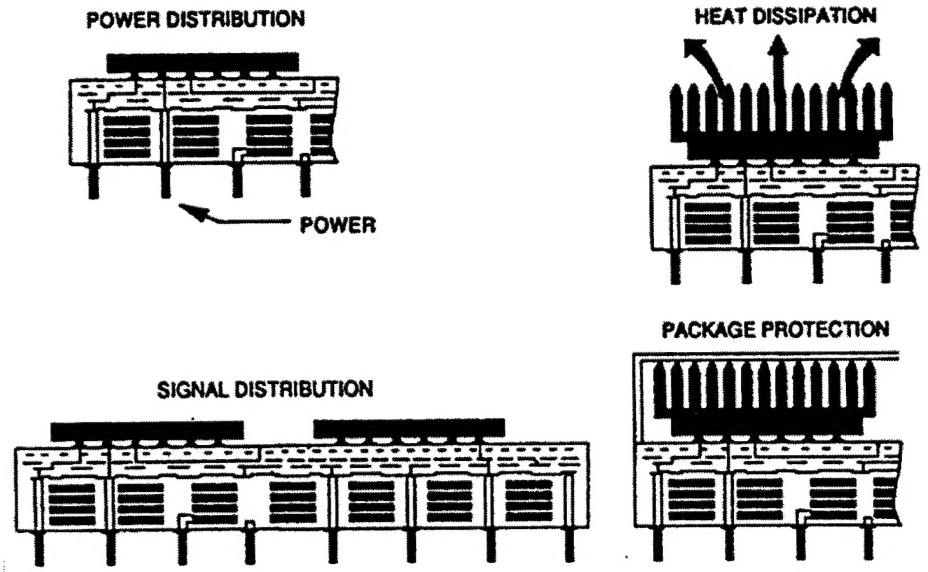

Figure 2. Packaging functions.

- ***Thermomechanical compatibility***: Thermal expansion differences between the die and the package as well as between the different packaging components result in stresses during assembly as well as during operation that can result in the failure of the package or the device. The thermal expansion mismatch between the die, the substrate, and other packaging components should be small at all temperatures to minimize thermal stresses. Thermal expansion mismatch may increase with temperature and can aggravate the thermal stress problem.
- ***Chemical compatibility:*** Metallization should not react with the die and the substrate at assembly and service temperatures. Electromigration of conductors must be prevented or minimized to prevent failures by shorting. The temperature coefficient of resistance should be as small as possible within the intended temperature range.
- ***Hermeticity:*** The package should have atmospheric integrity to protect the die from environmental elements.
- ***Simplicity, size, and weight***: The package should be readily manufacturable, small in size, and lightweight for aircraft and space applications. The package material properties dictate the form factor.

3. HIGH-TEMPERATURE PACKAGING MATERIALS

3.1 Substrates

A survey of current substrate materials for high temperatures, including ceramics and glasses, is presented in Table 1. BeO is not considered as a viable candidate due to its toxicity and health hazards. Glass and glass ceramics suffer from low thermal conductivity and weak mechanical properties, while SiC suffers from low dielectric strength, high dielectric constant, and high dissipation factor, which can impact high-frequency or high-speed device operation. On the other hand, hot-pressed BN has a significant CTE mismatch with both Si and SiC in addition to its poor mechanical properties. Its chemical stability in oxidizing environments at high temperatures is also questionable. When compared to AlN, Al_2O_3 has a lower thermal conductivity and a higher dielectric constant. The temperature rise can cause Al_2O_3 to lose its already low thermal conductivity, while AlN still shows a thermal conductivity of over 100 W/m-K at 400°C as shown in Figure 3. Al_2O_3 has a CTE of 7.8×10^{-6}/°C, which significantly differs from that of SiC (3.7×10^{-6}/°C). The CTE mismatch causes thermal residual stresses that then lead to device failures. This problem can be totally eliminated if one uses AlN, since its CTE is very close to that of SiC as illustrated in Figure 4.

As the temperature rises, the dielectric constant of oxide ceramics increases rapidly as shown in Table 2. However, because AlN is mostly covalent, the dielectric constant and dielectric loss rise little with increasing temperature as shown in Tables 2 and 3, respectively.

In summary, AlN appears to be an ideal candidate for high-temperature packaging applications over 600°C. It is produced in large sizes (up to 9 in. × 9 in.) and thus can be utilized as the printed circuit board itself with proper metallization. Some of the important advantages of AlN include the following:

- A CTE that closely matches those of Si and SiC, which minimizes thermal stresses.
- High thermal conductivity, which decreases only slightly with increasing temperature.
- Good thermal shock resistance and environmental stability at high temperatures.
- Nontoxicity (unlike beryllia).
- High electrical resistivity.
- High mechanical strength.
- Chemical inertness at high temperatures.

Table 1. Material property comparison.

	Si	SiC	Al_2O_3	AlN	BeO	SiC	Borosilicate Glass	BN-hp
Density, g/cm^3	2.3	3.21	3.75	3.31	2.90	3.21	2.13	25
Hardness, GPa	11.5	24.0	19.0	12.0	12.0	24.0	-	2.5
Strength, MPa	250	450	350-400	350-400	200-250	450	70	53
Elastic modulus, GPa	130	470	397	320	345	420	195-265	43
Thermal conductivity, W/m·K	150	300	25	200	250	70	4.0	25
Thermal expansion coefficient, ppm/°C	3.5	3.7	7.2	4.1	8.0	3.7	3.25	0.3
Resistivity, ohm-cm	--	--	$>10^{14}$	$>10^{14}$	$>10^{14}$	1	10^{11}	10^{11}
Dielectric constant (@ 1 MHz)	11.0	42	9.4	8.9	7.0	42	4.6	4.1
Dissipation factor (@ 1 MHz)	0.09	0.05	0.0004	0.0005	0.0003	0.05	0.002	0.0045
Dielectric strength, kV/mm	--	--	15	15	10	0.7	--	--

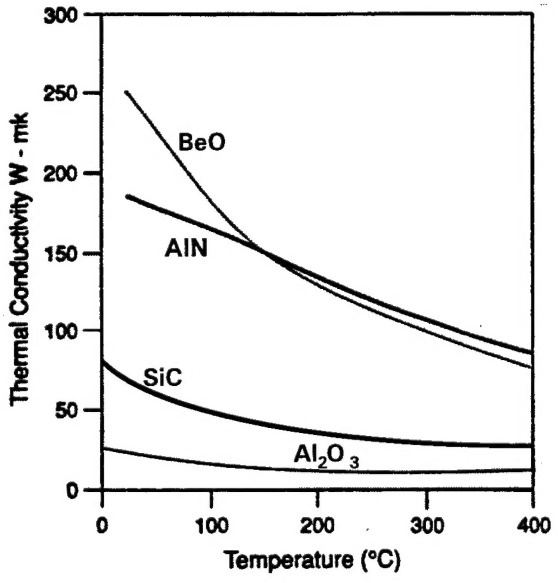

Figure 3. Thermal conductivity of commercial BeO, AlN, SiC, BeO, and Al_2O_3 (Blum, 1989).

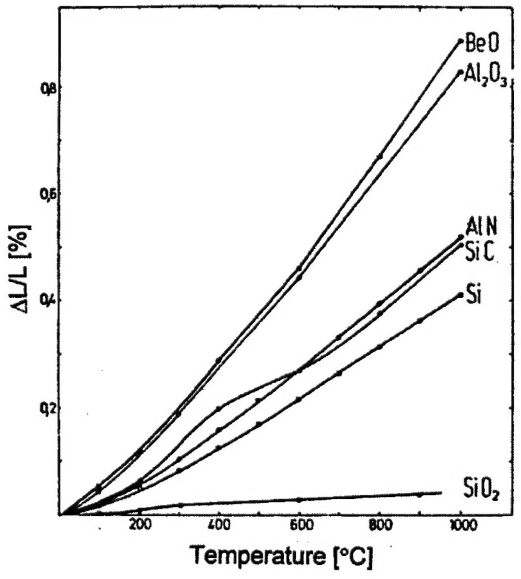

Figure 4. Thermal expansion of AlN and Al_2O_3 in comparison to that of SiC and Si (Werdecker and Aldinger, 1984).

Table 2. Dielectric constants for various materials as a function of temperature.

Material	Kr	Kt/Kr		
	23°C	1000°C	1200°C	1400°C
Fused silica (high purity)	3.82	1.02	1.03	1.04
Spinel ($MgAl_2O_4$)	8.2-8.4	1.19	1.25	--
Boron nitride	4.2-4.5	1.05	1.07	1.09
Silicon nitride	7.5-8.8	1.08	1.11	1.16
Alumina	9.5-9.8	1.15	1.21	1.27
Beryllia	6.6-6.8	1.16	1.24	1.32
Aluminum nitride	8.3-8.5	1.10	1.13	---

Table 3. Dielectric loss (tangent δ) of AlN as a function of temperature.

Temperature (°C)	Tan δ
23	0.0011
250	0.0017
523	0.0023
805	0.0050
893	0.0120
920	0.0190
950	0.022
1000	0.032

3.2 Metallization

When a metal on a substrate is exposed to high temperatures, several things can happen:

- The reactivity of metal with its surroundings, i.e., the substrate, increases. Such reactivity could be limited to interdiffusion or could lead to a chemical reaction resulting in new compound formation.
- The resistance of metal increases even if there is no significant interdiffusion or reaction with the surroundings. Reduction in conductivity can cause additional heat generation and loss in the ability to remove heat, where the metals are used as a thermal path in circuit board applications. Declining conductivity can also contribute to increased time delay and performance loss in high-speed applications.
- The electromigration induced by the flowing current is enhanced due to increased self-diffusion. Electromigration can lead to failures by forming open circuits.
- The difference between the CTE of the metallization and that of the substrate increases with increasing temperature. CTE mismatch causes thermal stresses that lead to failures.

The reactivity of the metal, electromigration, grain growth, and hillock growth are influenced by the self-diffusion in the metal and between the metal and its surroundings. Diffusion in metals is related to the melting point and the crystallinity of the metal. The higher the melting point, the lower the diffusivity. The self-diffusion in a metal is related to its melting point by the following empirical relationship:

$$Q_{S\text{-}D} = 34T_m$$

where Q is the activation energy in calories per mole and T_m is the melting point in degrees Kelvin. In package construction, all materials used must have melting points well above 600°C. The materials must also have a hierarchy of melting temperatures, as shown in Figure 5, that permits the desired sequence of assembly, i.e., die attachment then sealing and lid attachment. However, this hierarchy does not need to be rigid, because some attachment steps may involve only local or transient heating.

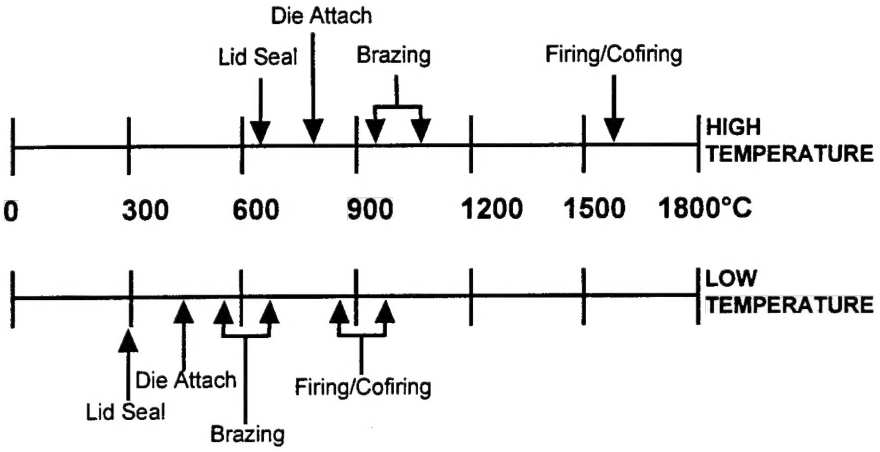

Figure 5. Schematic of process hierarchy in packaging systems.

3.2.1 Substrate Metallization

An ideal high-temperature metallization should have the following properties:

- High melting point over 600°C.
- Low electrical resistivity.
- Low-temperature coefficient of resistance.
- Matching CTE with AlN.
- High bond strength between metallization and AlN.
- High thermal conductivity.

The large CTEs of metals ($10–17\times10^{-6}$/°C) can give rise to large thermal stresses, which can cause device failures. Refractory metals such as W, Mo, Ta, Zr, and Ti may be suggested. However, W and Mo do not adhere to AlN and require a protective coating to prevent oxidation. Ta, Zr, and Ti show some promise, as thermodynamic calculations suggest the formation of aluminides that can form an interface between AlN and these metals.

Refractory metal silicides and borides represent the best performance/compromise mix for applications at 600°C and above. These may not be ideal solutions to the problem but represent rather the most promising approach. Some of the candidates are refractory silicides and borides of tungsten, tantalum, titanium, and molybdenum, as listed in Table 4. Refractory silicides and borides have CTEs

Table 4. Electrically conductive materials.

Material	Resistivity (μΩ-cm)	Temperature Coefficient of Electrical Resistance ($\times 10^{3}$/°C)	CTE ($\times 10^{-6}$/°C) @ 27°C	Thermal Conductivity (W/m·K)	Melting Temperature (°C)	Lowest Eutectic Temperature (°C)
Cu	1.5	6.8	17	398	1083	
Au	2.0	4.0	14	315	1063	
Al	2.4	4.29	25	237	660	
W	4.8		4.5	178	3400	
Mo	5.0		5.0	138	2620	
Ni	6.0	6.9	13	91	1453	
Co	6.2	6.04	12	100	1495	
Pd	9.8	3.77	8.5	71	1550	
Pt	10.6	3.9	9.0	73	1770	
Ta	12.2	3.83	6.5	57.5	2980	
Nb	12.5		7	53	2467	
Ti	42.0		8.5	22	1640	
$TiSi_2$	≈ 6.0	4.63	7.5		1500	1330
$CoSi_2$	≈ 6.0		7.5	54	1326	1195
$NbSi_2$	6.3		7.0		1950	1295
$TaSi_2$	8.5	2.24	8.3		2200	1385
$MoSi_2$	22	6.38	5.1	49	2030	1410
WSi_2	12.5	2.91	8.3		2165	1440
ZrB_2	7	2.3	7.6	58	3245	
TiB_2	9.0	2.0	6.8	64	2980	
NbB_2	12		6.5			
ZrN	13.6	2.0	7.0			
TiN	21.7	2.48	6.6	13	2950	
Diamond	$>10^{9}$		0.8			

(5–7×10^{-6}/°C) that match both AlN and SiC, thus minimizing potential thermal residual stress problems. They also have low electrical resistivities: 6 microohm-cm for $CoSi_2$ and $TiSi_2$ and 12.5 microohm-cm for WSi_2, as shown in Figure 6. These materials can be deposited by conventional CVD techniques and patterned using conventional lithographic techniques on AlN.

3.2.1.1 Metal Silicides

The resistivity of silicides is the single most important factor in considering them for use as metallization in substrates and in integrated circuits. The resistivity of the silicides is controlled by their stoichiometries. Silicon-rich disilicides of any given element exhibit the lowest resistivity.

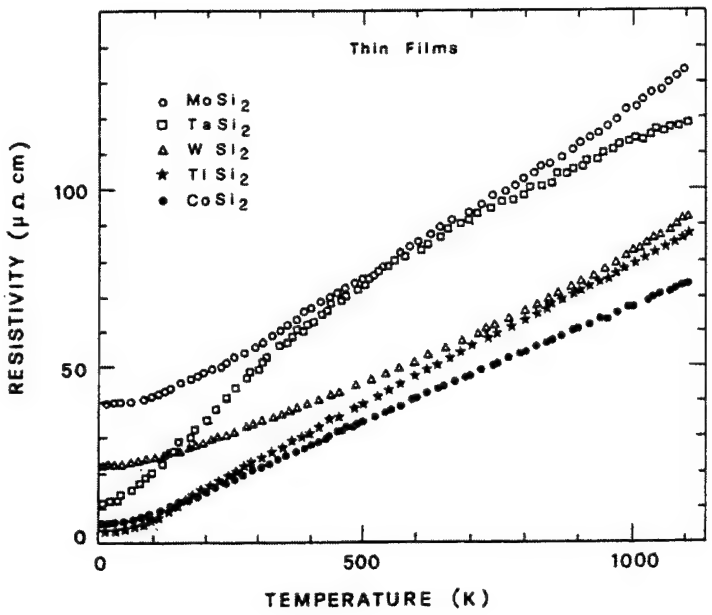

Figure 6. Electrical conductivities of silicides (Nava et al., 1993).

Table 5 lists the resistivities of several disilicides. A range of resistivities is shown in each case. The variation in the resistivities is the result of variability in preparation of the silicides. The variability is caused by purity (especially oxygen contamination), stoichiometry, and the degree of crystallinity. Oxygen increases the resistivity significantly. The role of oxygen in controlling the resistivity of silicides is not clearly understood. Oxygen is, however, expected to bond to metal (W, Ta, Ti) or silicon effectively, reducing the charge carrier density and leading to an increase in resistance. Murarka (1983) has shown that the resistivity of as-deposited amorphous silicides increases as the Si/Me ratio increases. After sintering, the resistivity value goes through a minimum for a given Si/Me ratio; for example, in the Ti-Si system the resistivity is at a minimum for Si/Ti = 3 and higher for Si/Ti ratios lower or higher than 3.

As the annealing temperature increases, the sheet resistivity decreases. This is attributed to the crystallization and grain growth during annealing, since grain boundaries can scatter charge carriers very effectively increasing the resistivity.

Murarka (1989) reported that a small amount of excess silicon (Si/W = 2.2) in WSi_2 led to the formation of metastable hexagonal WSi_2 at temperatures below 700°C and increased the sheet resistivity. Over 700°C, tetragonal WSi_2 was formed, accompanied by a decrease in sheet resistivity.

The Phase I work also showed that sheet resistivities of WSi_2, $TiSi_2$, and $NbSi_2$ decreased significantly with increasing annealing temperature. However, the annealing process was not optimized.

The electrical behavior of the disilicides is like that of a metal, i.e., its resistivity, ρ_{tot}, follows Matthiessen's rule:

$$\rho_{tot} = \rho_i + \rho_{res}$$

where ρ_i is the intrinsic resistivity and ρ_{res} is the residual resistivity. ρ_i depends on the density of electron states at the Fermi level, as well as on the mass and bulk modulus of the material. ρ_{res} depends on defects in the microstructure including grain boundaries, impurities, second phases, and strain in the crystal lattice.

Intrinsic room-temperature resistivity for WSi_2 and other refractory disilicides is given in Table 6.

Table 5. Resistivities of various disilicides (Murarka, 1983).

Silicide	Formed by Starting From	Sintering Temperature (°C)	Resultant Resistivity (μΩ-cm)
$TiSi_2$	Metal on polysilicon Cosputtered alloy	900 900	13 - 16 25
$ZrSi_2$	Metal on polysilicon	900	35 - 40
$HfSi_2$	Metal on polysilicon Cosputtered alloy	900	45 - 50 60 - 70
VSi_2	Metal on polysilicon	900	50 - 55
$NbSi_2$	Metal on polysilicon	900	50
$TaSi_2$	Metal on polysilicon Cosputtered alloy	1000 1000	35 - 45 50 - 55
$CrSi_2$	Metal on polysilicon	700	~600
$MoSi_2$	Metal on polysilicon Cosputtered alloy	1100 1000	~90 ~100
WSi_2	Cosputtered alloy	1000	26 - 70
$FeSi_2$	Metal on polysilicon	700	>1000
$CoSi_2$	Metal on polysilicon Cosputtered alloy	900 900	18 - 20 25
$NiSi_2$	Metal on polysilicon Cosputtered alloy	900 900	~50 50 - 60
$PtSi_2$	Metal on polysilicon Cosputtered alloy	600-800	28 - 35
Pd_2Si	Metal on polysilicon	400	30 - 35

Table 6. Intrinsic room-temperature resistivity of various silicides (Murarka, 1989).

Silicide	ρ_i (μΩ-cm)
$MoSi_2$	18, 20
$TaSi_2$	26, 40, (26⊥′, 42❹♦)*
$TiSi_2$	11, 13
WSi_2	7
$CoSi_2$	10
$NiSi_2$	20

*⊥′ and ❹♦ refer to directions perpendicular and parallel to ⟨100⟩ direction. $TaSi_2$ thus exhibits anisotropic resistivity.

As a consequence, a number of questions arise:

- What is the ultimate resistivity achievable in WSi_2? What is the resistivity trade-off in a WSi_2-W_5Si_3 mixture, which is easy to obtain?
- Can a low resistivity be obtained at lower annealing temperatures in a reasonable time?
- Can the stress induced in the thin film due to coefficient of thermal expansion mismatch between WSi_2 and SiC and AlN be annealed out?

3.3 Interconnect Materials

Metallic conductors are used in metallization and in interconnects in multi- and single-layer electronic packages. In regular electronics, most electrical interconnects are made by microwelding (wire bonding), brazing (lid sealing), and soldering (die attach).

High temperatures impose additional requirements on the materials and processes. As a rule of thumb:

- The melting temperature of the metal should be at least 1.5 times higher than the operating temperature to prevent any diffusion-related problems such as creep and electromigration.
- The metals in contact with each other should not form intermetallics at operating temperatures.

These considerations impose many limitations and eliminate some of the commonly used metals, such as silver (T_m = 961°C), as a candidate. Package elements posing the most concern are wires, wire bondings, die attaches, and to some degree, conductor lines (circuit traces).

Wire and wire bondings are the most critical because of the formation of the intermetallic phases at the bond pad. For example, in the gold-aluminum system, aluminum-gold intermetallics rapidly form over 175°C ("purple plague") and can cause failures through the Kirkendall voiding process. Therefore, wire and bond pad materials should not form intermetallics and preferably should be of the same material. The gold-gold system may be a candidate; however, creep may be a problem. Gold-nickel and palladium-nickel systems for the wire bonding process should be explored.

Mechanical die attachment is achieved by mounting the chip, back-side down, with glass, epoxy or metals onto the substrate. Packages intended for room-temperature applications use tin-lead solder or polymers as die attaches. However, solders are subject to low cycle fatigue, creep below 200°C, and even melting in some compositions.

In packages intended for use above 200°C, die attach is achieved by using a gold-silicon eutectic (T_m = 370°C) or silver-filled, low-melting-point glasses (T_m = 400-450°C). Once formed, the gold-silicon eutectic results in either a silicon-rich or gold-rich alloy, resulting in a new softening point well above the eutectic temperature. Thus, with proper alloy control, a gold-silicon eutectic can provide effective die attaches above 400°C. However, other nonintermetallic-forming binary alloy systems, such as Cu-Ni, Au-Cu, and Au-Ni, with suitable melting temperatures should be investigated as die attach materials. Low-melting-point glasses are useful up to 350°C. It is possible to use glasses with softening points above 600°C for the die attach, however, at the expense of package thermal conductivity.

Since the actual package design parameters and package form factors are not known, lead and lead frame materials cannot be investigated in detail. Alloy 42 and copper-clad-molybdenum are expected to work well, not only because of their high temperature resistance but also their matching thermal expansion coefficients ($4–5\times10^{-6}$/°C) to those of SiC and AlN. Table 7 (adapted from Charles and Clatterbaugh, 1994) summarizes packaging considerations for high-temperature operations.

After a semiconductor wafer such as silicon, gallium arsenide, or silicon carbide is cut into individual components (chips or die), one of the first operations in assembly is the chip attachment (die attach) to the metallized substrate. Another critical operation in packaging the semiconductor die is making

Table 7. Packaging components for high-temperature operations.

Temperature Range	Devices	Substrates	Housing	Die Attach	Interconnect	Metallizations
Up to 200°C	Silicon, GaAs	Organics (polyimide), ceramics, glasses	Plastics, metals, ceramics	Epoxy, solder, eutectic, glass	Wire bonding, TAB, flip chip	Copper*, gold, aluminum
Up to 400°C	GaAs	Ceramics, semi-conductors	Ceramics, metals (welded or brazed)	Eutectic, glass	Wire bonding (Al/Al and Au/Au)	Copper*, gold, aluminum, metal silicides
Up to 600°C	GaAs, wideband gap ma-terials, SiC	Ceramics, semi-conductors	Ceramics, metals (welded or brazed)	Eutectic, glass?	Wire bonding (Au/Au and Ni/Ni)	Copper*, gold, metal silicides

*With Au coating to protect from oxidation.

the electrical interconnections between the die and the package. Fine leads connect active microelectronic circuit chips to sturdy electrodes, which ultimately connect with external electrical components. Figure 7 shows a schematic of a die attached to a metallized substrate and wire bonded to the circuit traces on the substrate.

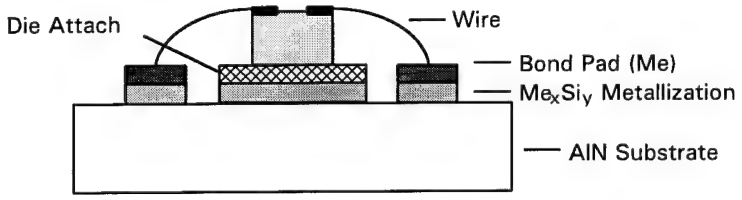

Figure 7. Schematic of die attach and wire bonding in a package assembly.

Even though there are other interconnection technologies, such as tape automated bonding (TAB) and controlled collapse chip connection (C4) or flip chip (FC), the wire bonding (WB) technique appears to be most suitable for the reasons listed below:

- Its ready adaptability to diverse metallizations and package styles.
- Its easy reworkability.
- Its amenability to visual inspection for bond quality screening.
- The ease with which nondestructive bond integrity tests can be performed.

All of these reasons are very important factors to consider in developmental work such as that proposed here. In addition, the extensive base of technical expertise and installed equipment in existing production lines is very critical for acceptance of developed technology by commercial vendors.

Several critical requirements must be satisfied for optimal selection of the materials for chip-to-package interconnections. The following specific requirements regarding the die attach material and wires and bond pads must be met.

3.3.1 Die Attach Material

From a design point of view, the ideal die attach material should have the following properties (Yang et al., 1993; Konsowski, 1993):

- Good adhesion to the die and the substrate so that the die can be attached without debonding and delamination.
- Self-resilience to provide good stress relaxation behavior so that induced internal stresses are reduced to low levels.
- High thermal conductivity so that heat dissipated from the power chip and the thermal expansion difference between the chip and the substrate can be minimized.
- An appropriate processing temperature and good thermal stability to fit into the process hierarchy shown in Figure 5.
- Corrosion resistance.
- Good reworkability.

The die attach materials include hard solders, soft solders, glasses, and organic adhesives. Soft solders and organics are not considered due to their low melting temperatures. Hard solders, non-silver brazes, and glasses (as a fallback) should be considered.

3.3.2 Wires and Bond Pads

Wire material should meet the following specific criteria in addition to the general requirements given in Section 3.2 (Gehman, 1980; Tummala and Rymaszewski, 1989):

- High electrical conductivity.
- Bondability to other material with available wire bonding methods.
- Chemical compatibility with the die and substrate silicide metallization. It should not form any intermetallic compounds with bond pad metallization.
- High creep resistance to prevent sagging.
- Self-resilience to relax internal stresses, which lead to failures of wires.
- High electromigration resistance.
- High strength and ductility for plastic deformation during bonding operations.
- Be formable into fine diameters, i.e., 25 μm.
- High corrosion resistance.

To define suitable pad materials, W-Si-Me ternary systems should be investigated, where Me includes Cu, Au, Ni, Pd, and their alloys. Then, wire materials compatible with chosen pad materials should be selected. Cu, Au, Ni, Pd, Au clad Cu, Au, or Pd clad Ni are among the candidates.

3.4 Silicon Carbide Integrated Circuit Metallization

Because of their low and metal-like resistivities, their high-temperature stability, and high electromigration resistance, the silicides are also primary candidates for Schottky barriers, ohmic contacts, gates, and interconnects in SiC ICs for high-power, high-temperature devices (Herndon, 1989). The desired properties of silicides for SiC ICs include the following:

- Low resistivity.
- Ease of fabrication.
- Patterning suitability.
- Stability in oxidizing ambients; oxidizability.

- Mechanical integrity, good adherence, and low stress.
- Surface smoothness.
- Stability throughout processing, including high-temperature sinter, dry or wet oxidation, gettering, phosphorous glass (or any other material) passivation, metallization, etc.
- Chemical compatibility with SiC and substrate metallization.
- Not a contamination source of devices, wafers, or working apparatus.
- Good device characteristics and lifetimes.
- For window contacts, low contact resistance and minimal junction penetration.

Even though the silicides are considered for the AlN substrate and chip back-side metallization in packaging, they are also suitable for SiC IC device metallization. However, their applicability to SiC ICs is beyond the scope of the current work and should be the subject of a separate investigation.

4. POTENTIAL APPLICATIONS

There are several industries that stand to benefit from high-temperature precision control systems to achieve performance improvements and competitive advantages. These high-temperature precision control systems require development of the high-temperature microelectronics devices and associated packaging. A summary of the applications for high-temperature electronics, their temperature ranges, required electrical circuits, radiation requirements, and device technologies is given in Table 8.

Perhaps the near-term and most significant applications for high-temperature microelectronics exist in the field of power electronics. Figure 8 summarizes power electronics technologies and potential applications for high-temperature microelectronics. These potential applications are briefly described and their estimated market potential is given below.

Table 8. Applications for high-temperature electronics (Dreike et al., 1994).

Application	Temperature Range	Types of Functions	Radiation Level	Device Technologies
Automotive - exhaust	55 to 250°C ~600°C	Sensors, amps, A/D, D/A, microcontrollers	None	SOI, SiC
Heavy equipment	55 to 250°C	Sensors, amps, A/D, D/A, micro-controllers power	None	SOI, SiC
Aeronautic	55 to >600°C	Sensors, A/D, D/A, micro-controllers power	Low (High Altitude)	SOI, SiC
Heavy vehicle brakes	-55 to 600°C	Sensors, A/D, microcontrollers	None	SiC
Well logging	-55 to 500°C	Sensors, A/D	Low, n & γ	SOI, SiC
Nuclear reactions and APT	25 to >1000°C	Sensors, amplifiers	n, p, & γ	SOI, SiC, vacuum microelectronics
Nuclear waste storage	25 to 150°C	Sensor, amplifiers telemetry	n & γ	SOI, SiC vacuum microelectronics
Radars	-55 to 200°C	RF Power	Low	SiC

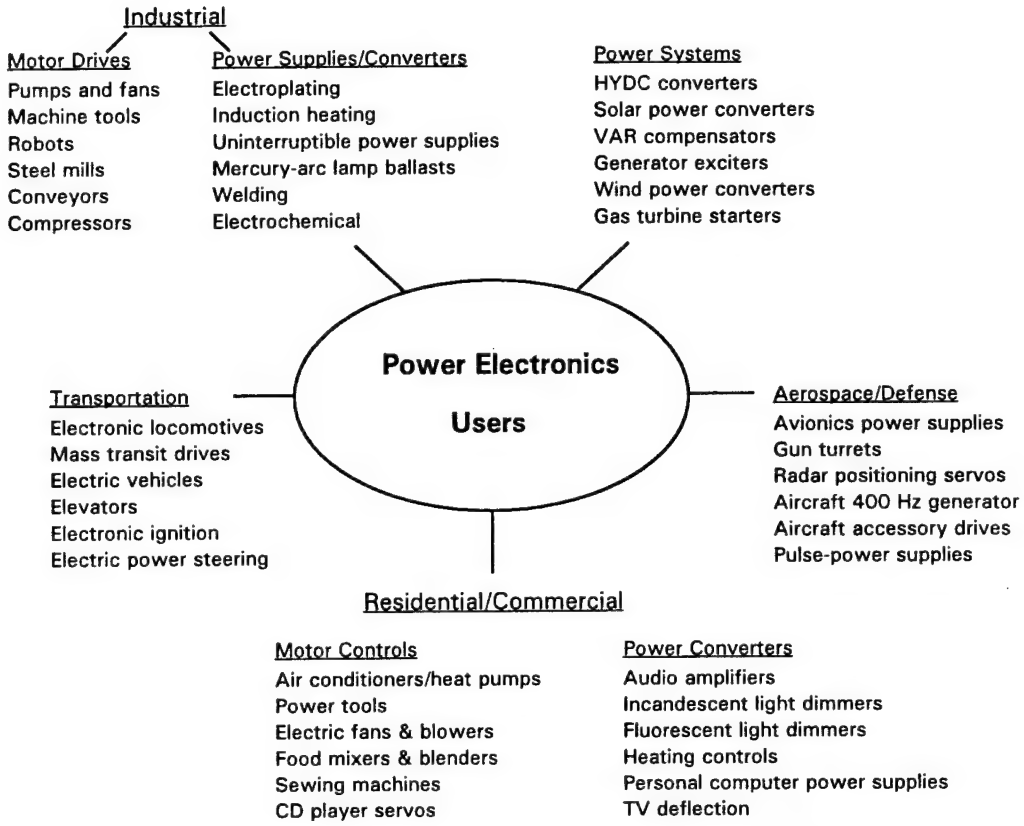

Figure 8. Power electronic technologies and applications.

4.1 Automotive

The largest number of automotive applications under consideration are for temperatures of less than 250°C. Some sources of information claim that 180-200°C is the highest temperature range of real interest, with the exception of antilock brake sensors in the 250°C range. Combustion sensors or sensors at the inlet of a catalytic converter could be very hot, up to 1000°C. Device lifetimes of about 3000 hours with very high reliability are required, with wide and frequent temperature cycles.

The size of the market for sensors to be applied in conventional or internal combustion engines for the automotive market is very difficult to gauge and is very price sensitive. However, with around 15 million automobiles and light trucks produced each year in the U.S. alone, this could be a very large market. The potential to reduce pollution and improve fuel economy by the use of more precise sensors and controls might justify relatively moderately priced components (a few dollars each). The needs of this market appear to be at the low end of the high-temperature range and also require relatively high levels of functionality, such as microcontrollers.

An automotive market that we have no information on is the electric vehicle market. This is potentially a very large market; 2 percent of the vehicles sold in California after 1997 must be nonpolluting, i.e., electric. This fraction is legislatively scheduled to rise 10 percent in the 2000s in California, and there is growing pressure to enact similar legislation in a number of northern states. This market requires power semiconductors for power conditioning up to about 100 kW (1 kW = 1.3 hp). There may be advantages to operating these devices at high temperatures; a few percent power dissipation is a lot of heat. The availability of devices that are smaller and that operate at higher junction temperatures or with better thermal conductivity might offer lighter, longer-range, and lower-cost vehicles due to reduced cooling system requirements. The market could be large enough to drive high-temperature electronics.

Brakes in heavy vehicles such as city buses reach temperatures of >500°C fairly routinely for brief periods. Associated brake wear is one of the major causes of accidents involving trucks. An ability to monitor and record brake temperatures would be a means of improving and monitoring truck safety. Antilock brake systems for these vehicles would also require high-temperature electronics. The size of this market is difficult to judge, but it could be substantial.

4.2 Heavy Equipment

The needs in heavy equipment are similar to those of automobiles, with the additional need for power devices that will operate in 160-250°C ambients. The heavy equipment requirements are for the next-higher temperature range above those for automobiles and include needs for power devices. Technical requirements of this market can easily be met by the high-temperature electronics developed for the automotive sector.

4.3 Aerospace Applications

Aerospace is a real and fairly substantial market for the 21st century. It is a high-value market where improvements in fuel efficiency, reliability, or safety can justify a substantial investment in controls. For high-performance military applications, the sensors, signal conditioning, and computers used in jet engines are cooled to below 125°C using the aircraft's fuel or are located remotely. In commercial aircraft, the electronics are positioned to be air cooled. Because of the high temperatures in jet engines, many sensors are located remotely from the real measurement points, for example, hydraulic fluid pressure sensors at the ends of isolation tubes. High-temperature sensors and signal processing electronics could increase aircraft reliability and performance by providing better response in turbine controls and by eliminating the weight of cooling systems and high-performance cabling.

Air Force MEA and NASA fly-by-wire programs are interested in replacing hydraulic aircraft controls with electrical controls (Reinhardt et al., 1995). Electronic sensors and controls are used in jet engines and might conceivably be embedded in the skins of supersonic aircraft. Supersonic flight also heats sensors in some areas of the aircraft skins.

A next generation of turbine controls is being developed using electronics that will operate at up to 300°C. There are presumably additional applications that could be addressed with 600-800°C devices. A high-speed civil transport (HSCT) for supersonic flight is being considered by NASA, Boeing, McDonnell-Douglas, Pratt & Whitney, and others. Controls are being contemplated for engine inlets that must operate in the 180-250°C range. Failures in electronics and cabling are one of the largest maintenance items in the supersonic Concorde. High-temperature electronics might be an enabling technology for HSCT.

GE is presently developing their UV photodiode (Brown and Ghezzo, 1995) as a part of a flame-out detection system that relies on high-temperature microelectronics. However, GE has difficulty with packaging SiC ICs in reliable, hermetic packages. GE would like to have high-thermal-conductivity AlN packages. The difficulty stems from the silver migration in the copper-silver brazes used for putting the package together. A solution would be to replace the silver-copper braze with electromigration-resistant gold-copper braze. However, current AlN metallizations are not compatible with the Au-Cu braze.

4.4 Well Logging

Fairly sophisticated sensors and electronics are used for logging the environment around drilling heads in oil, gas, and geothermal wells. The temperatures encountered in oil and gas drilling are 200-300°C, and geothermal temperatures range up to 500°C, as discussed by Traeger and Lysne (1988). Conventional electronics are used in these applications today by enclosing them in a dewar. The dewars and associated data loggers are a well-developed work-around for the high-temperature environment. However, if a

sufficiently broad range of components was available to upgrade current systems in a balanced fashion, there would be interest by this industry. The market is estimated at several million dollars per year, and the size of the market fluctuates substantially with interest in exploration.

AlliedSignal is one of the companies developing well logging sensors. QUEST has already established contact with AlliedSignal [P.O.C. Mr. Elliot Leyman, (201) 455-2670] to respond to their packaging needs.

4.5 High-Temperature Radiation Environments

These environments include nuclear reactors, the proposed accelerator-produced tritium (APT) facility, and nuclear waste storage tanks. Requirements for these applications are poorly defined, but they involve temperatures of up to several hundred degrees Celsius and essentially infinite gamma and neutron radiation doses. Incremental improvements in environmental hardness would presumably be valuable to the reactor industry. Waste storage tanks at the Hanford reservation contain millions of gallons of radioactive chemical wastes, at temperatures of up to perhaps 150°C. All of these applications could benefit from intelligent sensors and electronic processing capability in the hostile environments.

4.6 Radar and Communications

High-power phased-array radars can be performance-limited by problems with heat dissipation. There may also be applications in cellular telephone networks and other advanced telecommunications for RF devices that operate at a higher power density than present-day devices. This is an area in which improved device performance might leverage substantial improvements in the performance of a full system, for example, by eliminating the need for active cooling of a fighter aircraft radar. Airborne radars may also entail modest (<10 krad) total dose requirements as well as transient single-event upset and survivability requirements.

5. PROGRAM DESCRIPTION

5.1 Phase I Objectives

The objectives of the Phase I program were (i) to investigate the chemical compatibility of WSi_2, $TiSi_2$, and $NbSi_2$ with AlN and SiC, via diffusion couple studies; (ii) to prepare WSi_2, $TiSi_2$, and $NbSi_2$ thin films on AlN and WSi_2 on SiC; and (iii) to heat treat deposited films and to measure the electrical resistivities and characterize the interfaces between the films, AlN, and SiC using transmission electron microscopy.

5.2 Phase I Technical Approach

The overall approach to demonstrate the feasibility of the proposed concept included the following:

- Surface preparation of AlN substrates and SiC wafers.
- Calculation of the chemical equilibrium between AlN and the candidate silicides and between SiC and the candidate silicides.
- Formation of diffusion couples between AlN-WSi_2, $TiSi_2$, and $NbSi_2$-SiC.
- Characterization of diffusion couple interfaces to determine chemical compatibility.
- RF sputter deposition and heat treatment of WSi_2, $NbSi_2$, and $TiSi_2$ on AlN and of WSi_2 on SiC, the measurement of sheet resistivities, and the characterization of interfaces to determine thermo-mechanical compatibility.

The approach to the program was structured on sound scientific principles with industrial processing practices in mind. The tasks were carried out in a way that is compatible with current industrial electronic packaging production practices so that the process to be developed at the conclusion of this program can be readily scaled up for production. The work conducted under each task and the results are discussed below.

5.3 Phase I Tasks

The tasks were carried out in a way that is compatible with current ceramic package production practices; therefore, the processes developed during the program are readily adaptable for commercial production. The following tasks were performed during the proposed project.

5.3.1 Task 1. Diffusion Couple Studies

The chemical equilibria of AlN and SiC with WSi_2, $MoSi_2$, $NbSi_2$, $TiSi_2$, and $TaSi_2$ were calculated. AlN-WSi_2-SiC, AlN-$TiSi_2$-SiC, and AlN-$NbSi_2$-SiC diffusion couples were prepared and characterized by x-ray diffraction, scanning electron microscopy, and energy-dispersive x-ray microanalysis.

5.3.2 Task 2. Interconnect Material Deposition, Heat Treatment, and Interface Characterization

Aluminum nitride substrates were polished and cleaned before thin film deposition. WSi_2, $TiSi_2$, and $NbSi_2$ films were RF sputtered from commercially available targets. The deposited films were heat treated in argon. Sheet resistivities of the films were measured before and after the heat treatments. Thin films and interfaces were analyzed by transmission electron microscopy, electron microdiffraction and energy-dispersive x-ray microanalysis spectroscopy.

6. EXPERIMENTS, RESULTS, AND DISCUSSION

6.1 Task 1. Diffusion Couple Studies

Calculations were made of the chemical equilibrium of AlN and SiC with WSi_2, $MoSi_2$, $NbSi_2$, $TiSi_2$, and $TaSi_2$ up to 1000°C in an argon atmosphere. The calculations were performed with a commercial code (HSC chemistry) based on Gibbs' free energy minimization algorithm. Some of the results are given in Figure 9. The calculations showed that WSi_2, $MoSi_2$, and $TaSi_2$ did not react with AlN and SiC; $NbSi_2$ reacted with AlN at 800°C and with SiC at 500°C; while $TiSi_2$ reacted with both AlN and SiC at temperatures of 400°C. However, chemical equilibrium calculations do not provide any information on the kinetics of the possible reactions. With this fact in mind, and considering the electrical conductivities, we decided to prepare diffusion couples of AlN and SiC with WSi_2, $TiSi_2$, and $NbSi_2$. $TiSi_2$ and $NbSi_2$ were chosen due to their high electrical conductivities despite their reactions with AlN and SiC.

AlN substrates (QUEST Integrated, Inc.), 6H-SiC wafer (Cree Research, Inc.), and WSi_2, $TiSi_2$, and $NbSi_2$ blocks of 99.95-percent purity (Cerac, Inc.) were used in diffusion couple and thin film deposition experiments.

AlN-WSi_2-SiC, AlN-$TiSi_2$-SiC, and AlN-$NbSi_2$-SiC diffusion couples were prepared at 1000°C and 1200°C in an argon atmosphere. All AlN couples were characterized by x-ray diffraction and scanning electron microscopy. The results suggest that both WSi_2 and $NbSi_2$ appear to react with the yttrium-aluminum garnet (YAG) phase in the AlN substrate, as shown in Figures 10a and 10b. The lack of W and Nb peaks in Figures 10a and 10b suggests that WSi_2 and $NbSi_2$ do not react with AlN, while the presence of the Ti peak in Figure 10c is a strong indication of a reaction between $TiSi_2$ and AlN, as predicted by the chemical calculations.

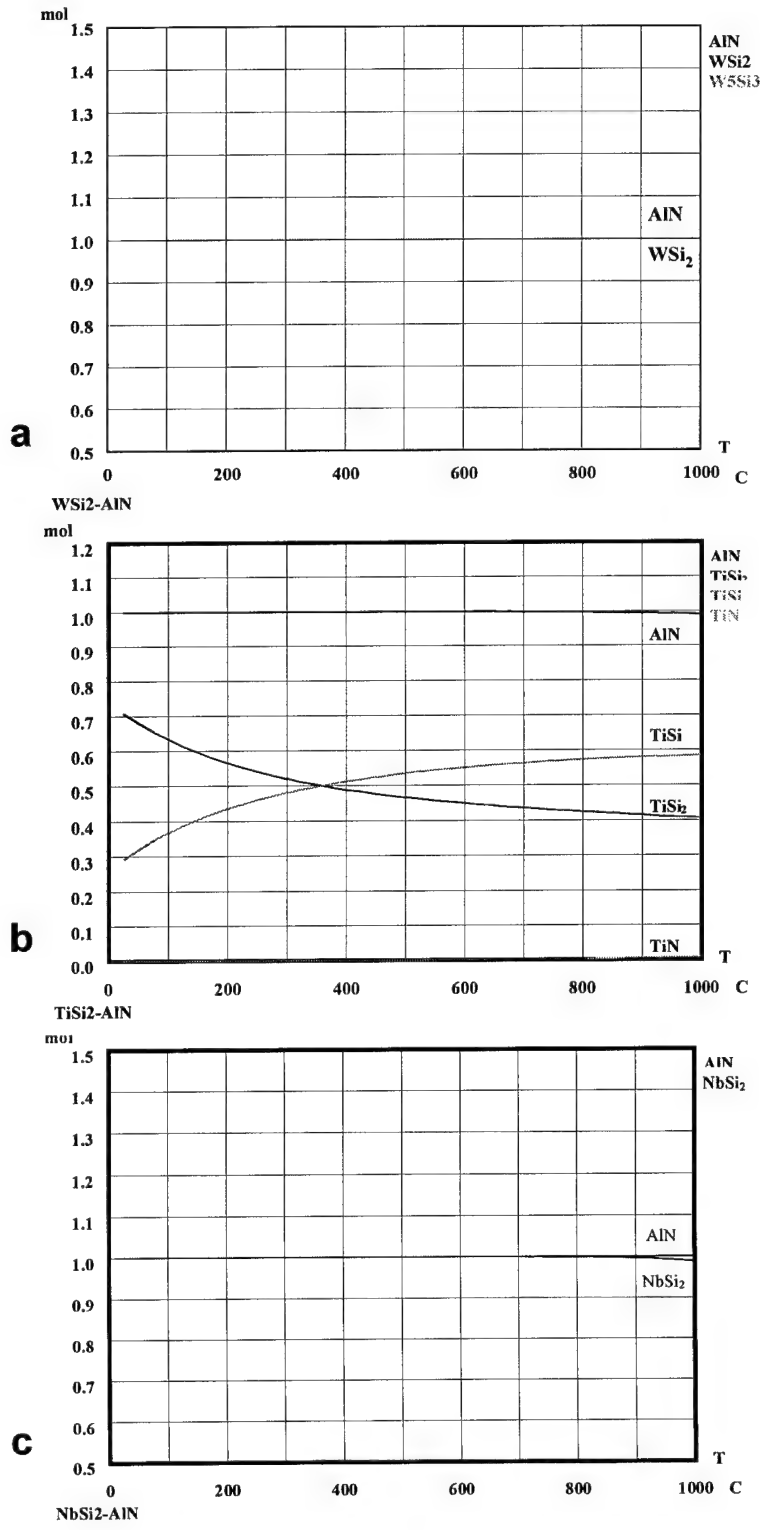

Figure 9. Graphical representation of chemical equilibrium calculations in (a) AlN-WSi_2, (b) AlN-$TiSi_2$, and (c) AlN-$NbSi_2$ systems.

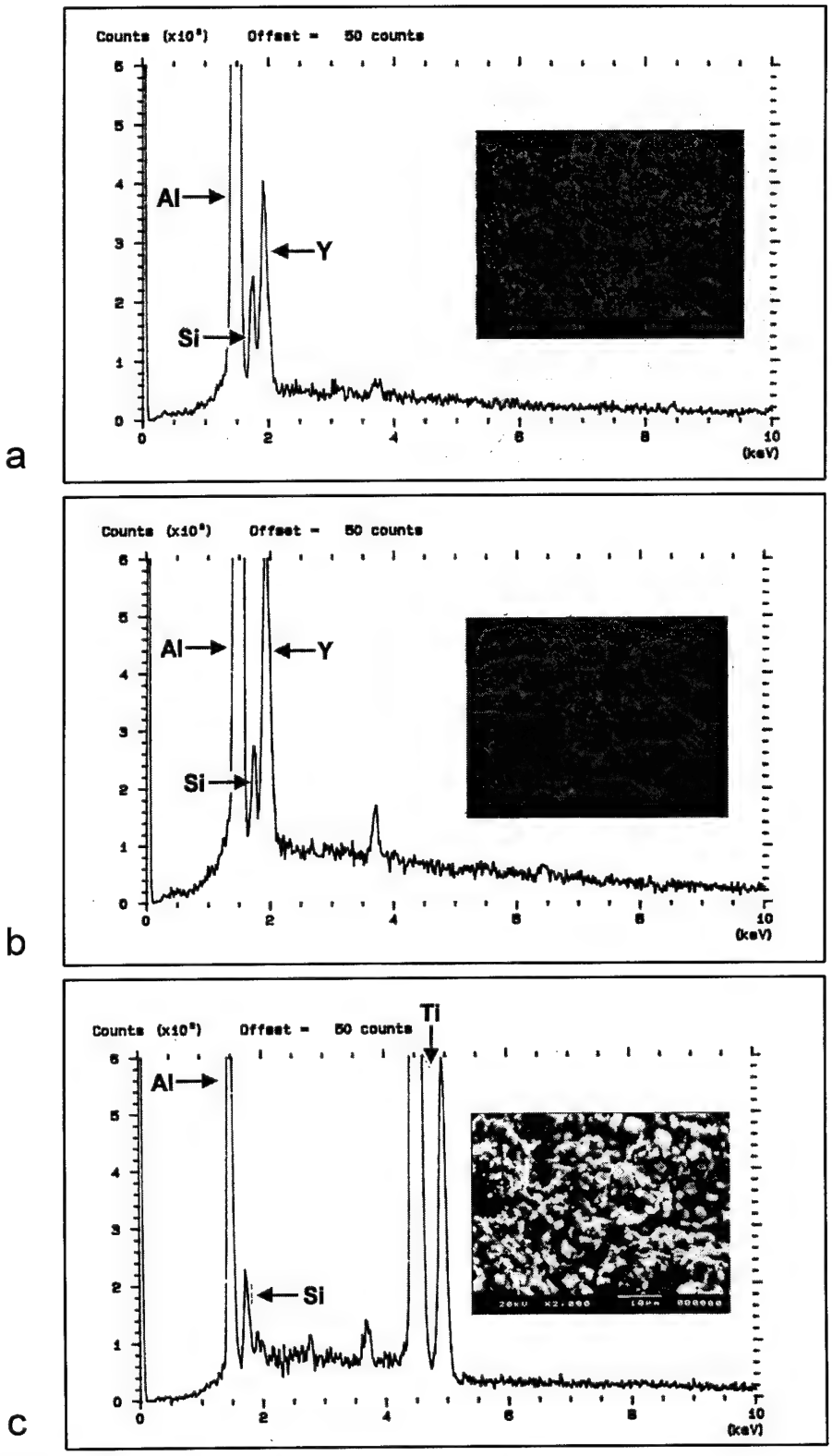

Figure 10. Micrographs and EDSs of AlN surface after diffusion couple experiments at 1200°C. (a) AlN-WSi_2, (b) AlN-$NbSi_2$, and (c) AlN-$TiSi_2$.

6.2 Task 2. Interconnect Material Deposition, Heat Treatment, and Interface Characterization

6.2.1 Aluminum Nitride-Silicides

Aluminum nitride substrates were polished to a surface finish of Ra = 0.050-0.075 micron. The substrates were ultrasonically cleaned in an acidic solution before thin film deposition. WSi_2, $NbSi_2$, and $TiSi_2$ thin films 0.7 micron thick were sputtered from commercially available targets. The deposited films were heat treated in argon at 900°C, 1000°C, and 1200°C for 1 hour. Sheet resistivities were measured by the four-point probe technique and are tabulated in Table 9. As expected, sheet resistivities decrease sharply with increasing annealing temperature. This behavior is attributed to crystallization and grain growth at high temperatures. As the number of grain boundaries (which act as electron-scattering centers) decreases, the electrical resistivity decreases also.

Table 9. Sheet resistivity of thin films.

Film	Sheet Resistivity, Ω/□			
	As Deposited	900°C	1000°C	1200°C
WSi_2	4.33	1.95	1.34	0.65
$TiSi_2$	4.27	3.5	2.0	2.0
$NbSi_2$	16.70	8.6	9.2	3.1

The values listed in Table 9 compare favorably to those of refractory metal (W or Mo) metallization. However, they can be improved upon further by modifying the target composition to adjust the film composition or by two-target sputtering followed by heat treatment to obtain the desired phases. These approaches will be explored in detail in the Phase II program.

A detailed analysis of the structure of the thin films and the interface regions was performed by transmission electron microscopy (TEM), electron microdiffraction, and energy-dispersive x-ray microanalysis spectroscopy (EDS). In all three cases, the silicide thin films displayed XRD patterns that were either loosely crystalline or completely amorphous. They did not have $MeSi_2$ stoichiometry but rather had Me_xSi_y stoichiometries.

A review of W-Si, Ti-Si, and Nb-Si phase equilibria shows that all have intermetallic silicide alloys either having a line composition or a finite compositional range with relatively high melting temperatures. These intermetallic alloys and their stoichiometry, crystal structure, and melting temperatures are listed in Table 10.

An XRD pattern taken from sputtered tungsten silicide films is displayed in Figure 11a. The figure shows two superimposed patterns: one from the reference AlN substrate and the other from a WSi_x-sputtered thin film (indicated as TF) on a polished AlN substrate. The AlN peaks are clearly visible being the high peaks (as indicated by the letter "a"). The XRD pattern from the silicide displays only weak peaks but with corresponding AlN peaks also.

The as-sputtered samples were subsequently heat treated to convert the amorphous layer of silicides into their crystalline forms and to investigate their phase instability and interface properties by microscopy and other physical measurement techniques. Although the application temperature is in the 600-700°C range, the samples were heat treated at a much higher temperature to crystallize the amorphous silicide phases and evaluate their stability. For this reason, the sputtered samples were subjected to heat treatments at 900°C, 1000°C, and 1200°C. Figure 11b displays one of the heat-treated samples, a WSi_2-sputtered sample that was heated to 900°C before being examined. In the XRD pattern, AlN as well as two forms of tungsten silicide, i.e., W_5Si_3 and WSi_2, are seen and are labeled, respectively, as b and c.

Table 10. Phase properties of selected silicides.*

	Structure	Solubility Range (at. %Si)	Melting Temperature (°C)
W-Si System:			
WSi_2	$C11_b$	line at 66	2164
W_3Si_5	$D8_m$	line at 63.5	2324
Ti-Si System:			
Ti_3Si	$P4_2/n$	line at 75	1170
Ti_5Si_3	$P6_3/mcm$	61-65	2130
Ti_5Si_4	$P4_12_12$	line at 55.5	1570
TiSi	Pmm2	line at 50	1480
$TiSi_2$	Fddd	line at 33.5	1330
Nb-Si System:			
Nb_5Si_3	D8m	line at 63.5	2484
$NbSi_2$	$D8_1$	line at 33.3	~1900

*Silicides stable from RT to their T_m; other high-temperature metastable silicides are not considered.

It is interesting to note that after heat treatment at 900°C for 1 hour, the amorphous layer was converted into a polycrystalline thin film. In this particular case of WSi_2 deposition (WSi_2 being the target material), both forms of W_xSi_y have formed, namely WSi_2 and W_5Si_3, as displayed in the XRD pattern in Figure 11b. From the pattern, it appears that the amounts of the two forms of silicides were about $W_5Si_3/WSi_2 = 3/2$ ratio.

6.2.1.1 Interfacial Phase Stabilities

Interfacial structures would best be examined by an imaging technique that has the capability of revealing the details of the amorphous and crystalline phase formation directly as well as providing capabilities of performing diffraction and spectroscopic analyses. TEM techniques were used, including bright field (BF) and dark field (DF) imaging, microdiffraction from areas as small as 50 Å diameter, and EDS for elemental analysis of the phases formed.

Samples that were heat-treated at 900-1200°C and contained silicide thin film on AlN substrate were prepared for TEM analysis using the cross-section method. For this, the AlN/thin film silicide samples were first cut into thin strips, and then two strips were glued together with an electron-radiation-resistant epoxy face-to-face on the silicide side. The sandwiched samples (with AlN substrate on the outside, silicide thin film on the inside, and epoxy in the middle) were sliced into thin sections about 200 μm thick, mechanically thinned down to 50 μm thick, and then ion-beam-milled down to an electron transparency of 1000 Å for analysis in an analytical TEM microscope (Philips 430T TEM/STEM) that operates at 200 kV accelerating voltage. The samples were placed in the TEM on a double-tilt, low-temperature holder. The following paragraphs give details of the analysis.

$NbSi_2$-deposited sample

Images of the cross-section sample in the BF and DF modes are shown in Figures 12a and 12b, respectively. As shown in the BF image, the AlN region is highly deformed and displays dislocations (the vertical "black" lines in the BF image and the corresponding bright lines in the DF image). This may be an indication that the interfacial reaction has caused the formation of new phase(s), which have

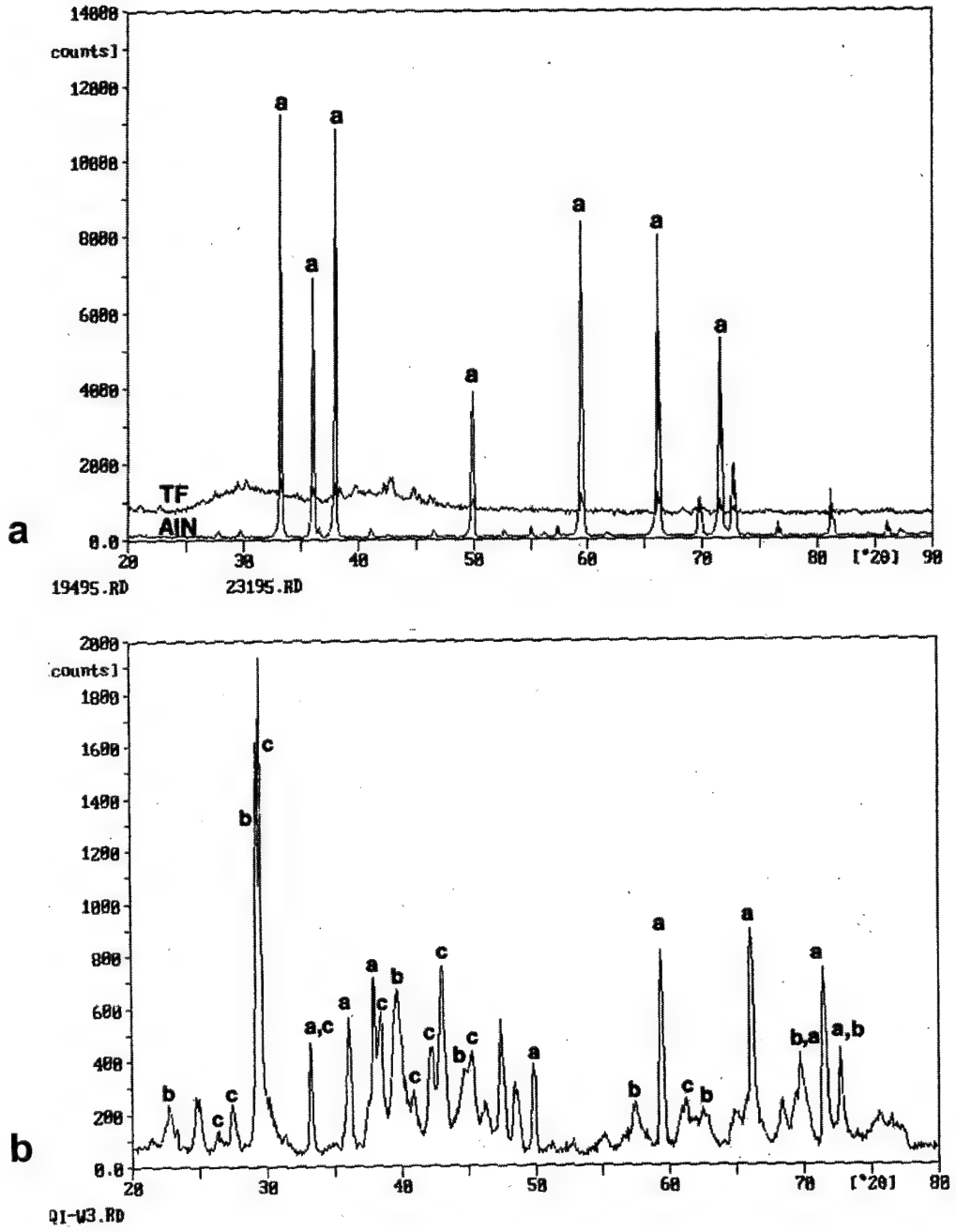

Figure 11. XRD patterns from the AlN substrate and the as-sputtered film of WSi_X. (a) The patterns from the substrate (indicated by AlN) display the peaks corresponding to the AlN phase (marked as "a"), while the pattern from the sputtered film displays only weak peaks; (b) Sample after heat treatment at 900°C. The peaks corresponding to AlN, W_5Si_3, and WSi_2 are marked by "a", "b", and "c", respectively.

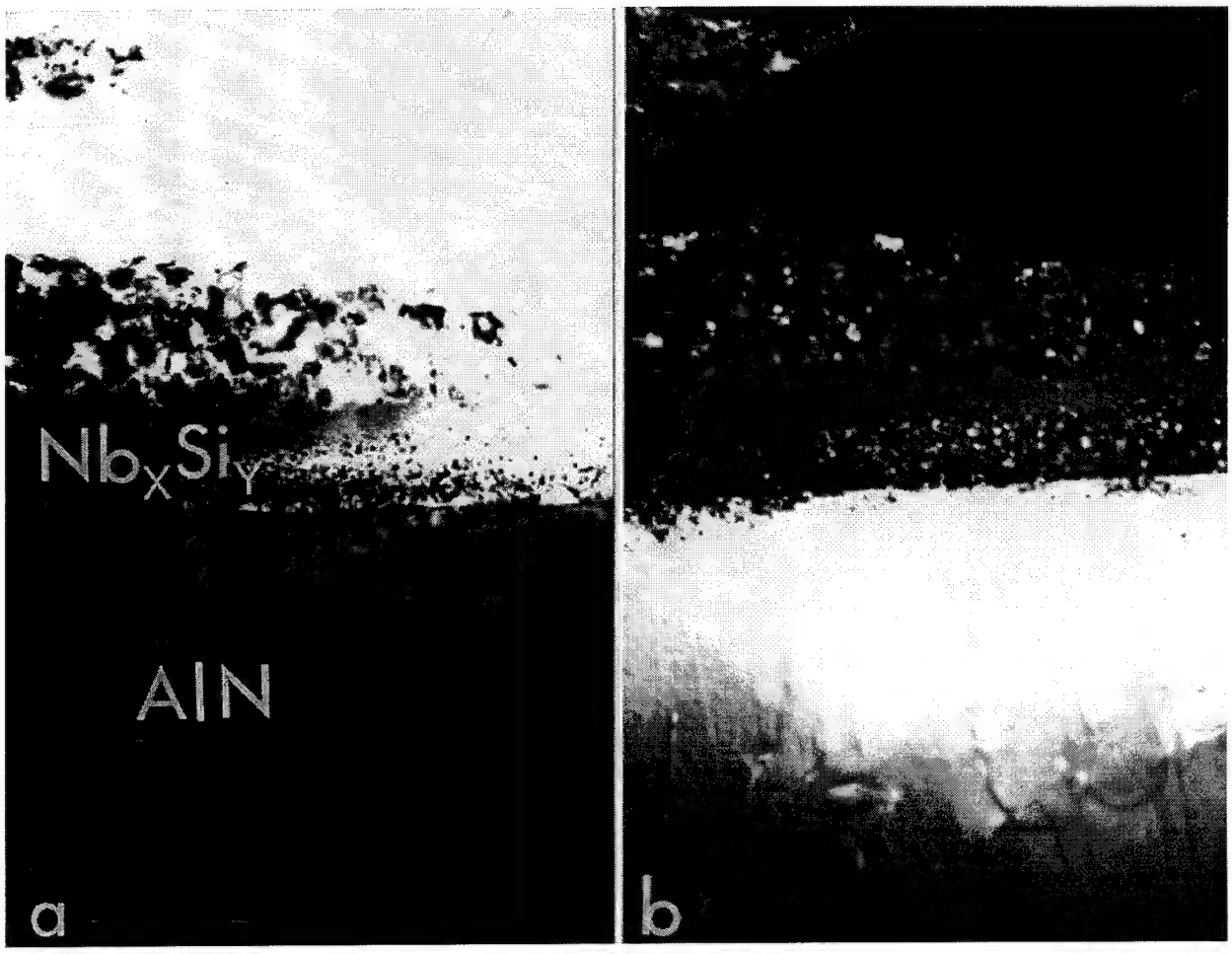

Figure 12. Images from the Nb_XSi_Y-AlN interface. (a) BF image and (b) DF image.

then induced stresses upon the temperature cycling during the heat treatment. The exact interface plane is not clearly deciphered but can be seen as a horizontal black line (from which the dislocations emanate). On the Nb_xSi_y side of the interface, the thin film appears to be polycrystalline giving a dark-bright contrast in the BF image and the corresponding DF image due to the diffraction contrast. Individual diffraction patterns, shown in Figure 13, recorded from the silicide regions correspond to various different phases in the Nb-Si phase diagram. The images in Figure 14 were taken from the same sample but at slightly different region at low and high magnifications to reveal the interface regions more clearly. A selected area diffraction pattern is also given, and it displays two types of superimposed patterns, one corresponding to the AlN phase and the other a ring pattern corresponding to the polycrystalline Nb_xSi_y patterns. The niobium silicide is probably not stoichiometric, and in the polycrystalline thin film there are probably several silicides present. For this reason, the composition of the silicide is referred to as Nb_xSi_y with varying x and y values depending on the type of the silicide (see Table 10). The selective area diffraction (SAD) pattern incorporates several of the Nb_xSi_y phases (which can only be identified with nanodiffraction analysis in which the electron probe is placed upon each individual crystallite of the silicide phase, as demonstrated in the case of the W_xSi_y-AlN sample as discussed below). A compositional profile across the interface was done by a small probe EDS analysis as discussed below.

Figure 15 gives the elemental analysis of the sample across the interface. The BF image shows the interfacial region that was used for the analysis, and the exact positions of the electron probe (about 100 Å in diameter) are shown as numbers from 1 through 5. The corresponding EDS spectra are displayed as 1 through 5. In the spectra, only the peaks corresponding to Al-K_α, Si-K_α, and Nb-K_α are displayed (Cu-K_α is a background count from the sample holder); N-K is far too small (401 eV) to be detected by the EDS spectrometer used in this work. What should be noticed are the changes of the relative heights of these peaks as the position of the electron probe changes. Although only an Al peak is seen at position 1, Nb and Si contributions are apparent at position 2. This region therefore appears to be a transition region with highly defective structure. At position 3, i.e., at the interface, the Si and Nb peak heights are much higher than at position 2, and the ratio gets even larger when the probe is placed well within the Nb_xSi_y region. The critical analysis is from the regions indicated as 2, 3, and 4, which progressively give higher Si and Nb contributions to the spectra than Al. It is possible, therefore, that there may be at least two types of phases that formed between the AlN and the silicide.

$TiSi_2$-deposited sample

The $TiSi_2$-AlN cross-section sample was also prepared for electron transparency for the interface stability investigation. Figure 16 displays a summary of the analyses completed on this sample. The images in Figures 16a and 16b were recorded at low and high magnifications, respectively, to reveal the structure near the interface. The regions that were clearly identified as AlN and $TiSi_2$ are indicated as such in Figure 16b. The rest of the area corresponds to a region between these two phases probably containing a number of Ti-Si intermetallic phases (see Table 10). Because of the complexity of the interfacial region, eight EDS spectra were recorded starting from the interior of the AlN phase to the central region in the cross-section sample (that corresponded to the epoxy). The EDS spectra are identified by the numbers 1 through 8 in Figure 16. Spectra 1 and 2, taken from the interior of the AlN and near the interface, both display Al peaks only (and a background Cu peak). However, starting from the position indicated by 3, both Si and Ti peaks increase. Regions 3 and 4 indicate a high amount of Si and Ti and a relatively low amount of Al. Region 5 displays minimal Al, Ti, and Si and seems to be an amorphous region in the form of a thin film. Regions 6 and 7 indicate an Si/Ti ratio increasing as one moves into the central region of the sample, indicating a stoichiometry increasingly weighted on Ti. Therefore, the ratios of Si/Ti are indicative of the various titanium silicides that can form in this temperature range (refer to the phase diagram). Finally, the EDS spectrum corresponding to position 8 displays predominantly Ti peaks and minimal Al and Si peaks, both of which are likely to be due to spurious x-rays. Therefore, we conclude that at the central region in the BF image in Figure 16 (i.e., the top surface of the titanium-silicide-deposited AlN sample), the phase corresponds to the stable metallic Ti.

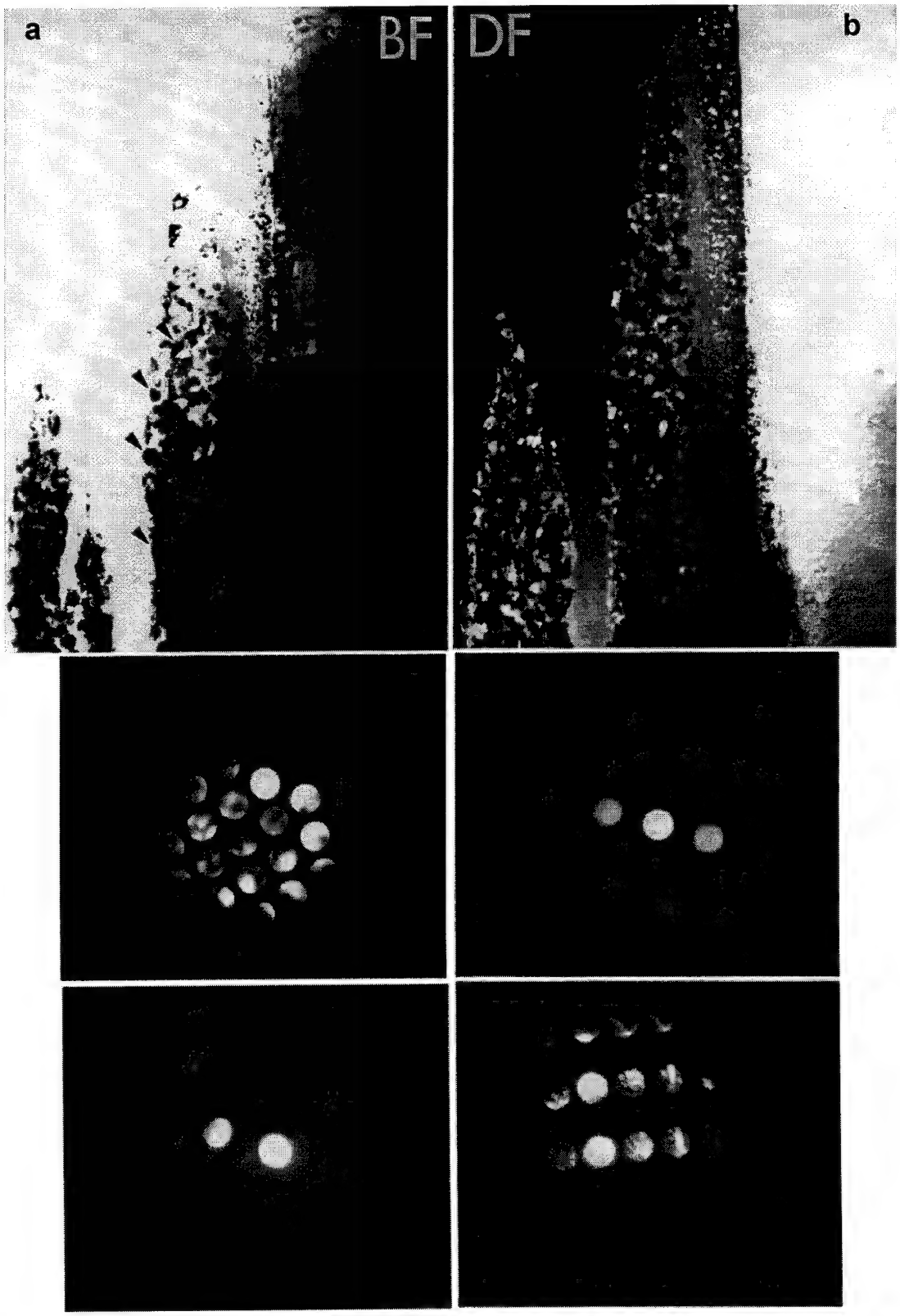

Figure 13. Images and nanodiffraction patterns recorded from the nanocrystalline regions in the silicide layer. (a) BF image and (b) DF image. The diffraction patterns correspond to different silicide phases between Nb and Si.

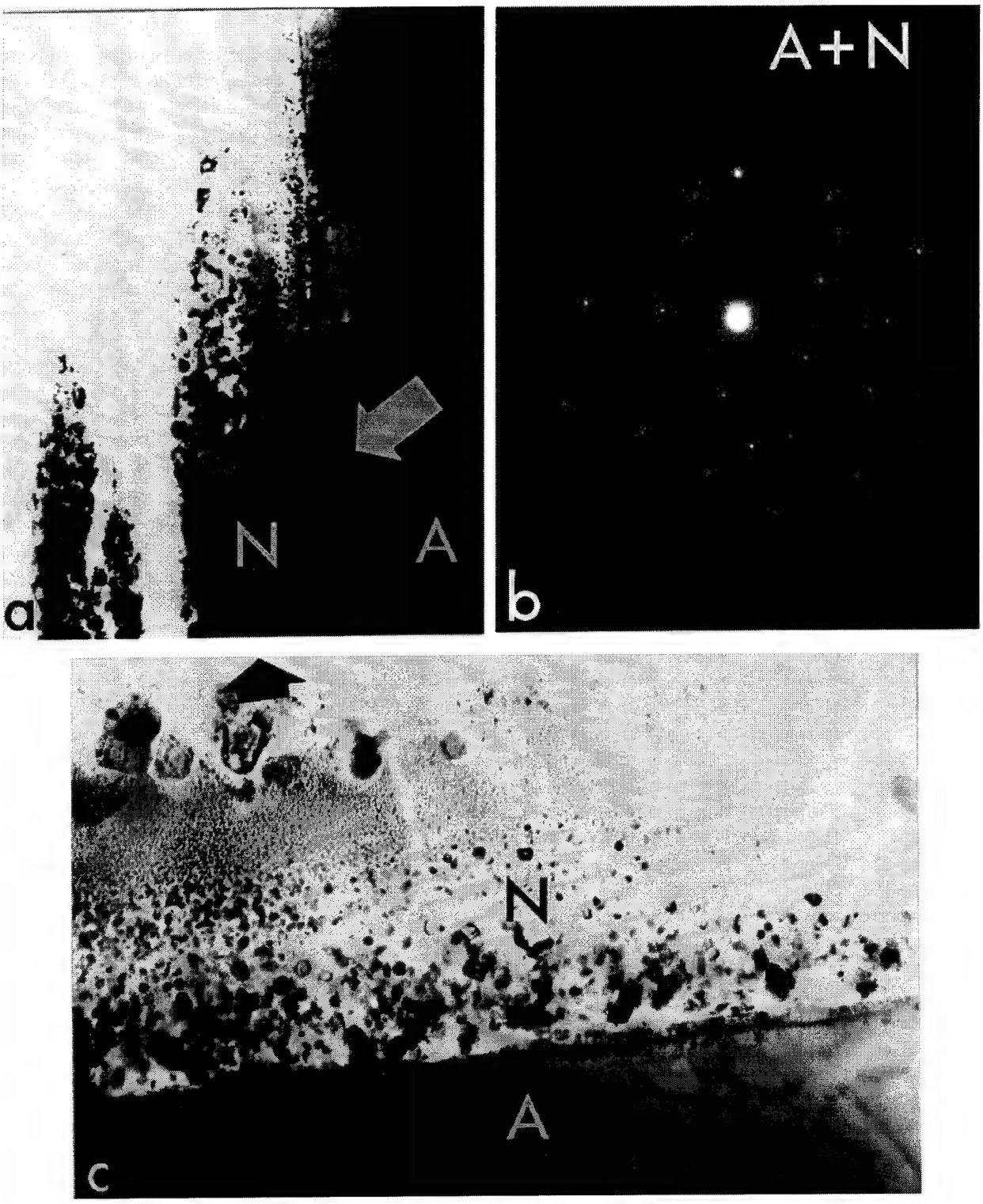

Figure 14. Nb_xSi_y-AlN sample. (a) Low-magnification image, (b) SAD pattern from the interface region, and (c) BF image at high magnification.

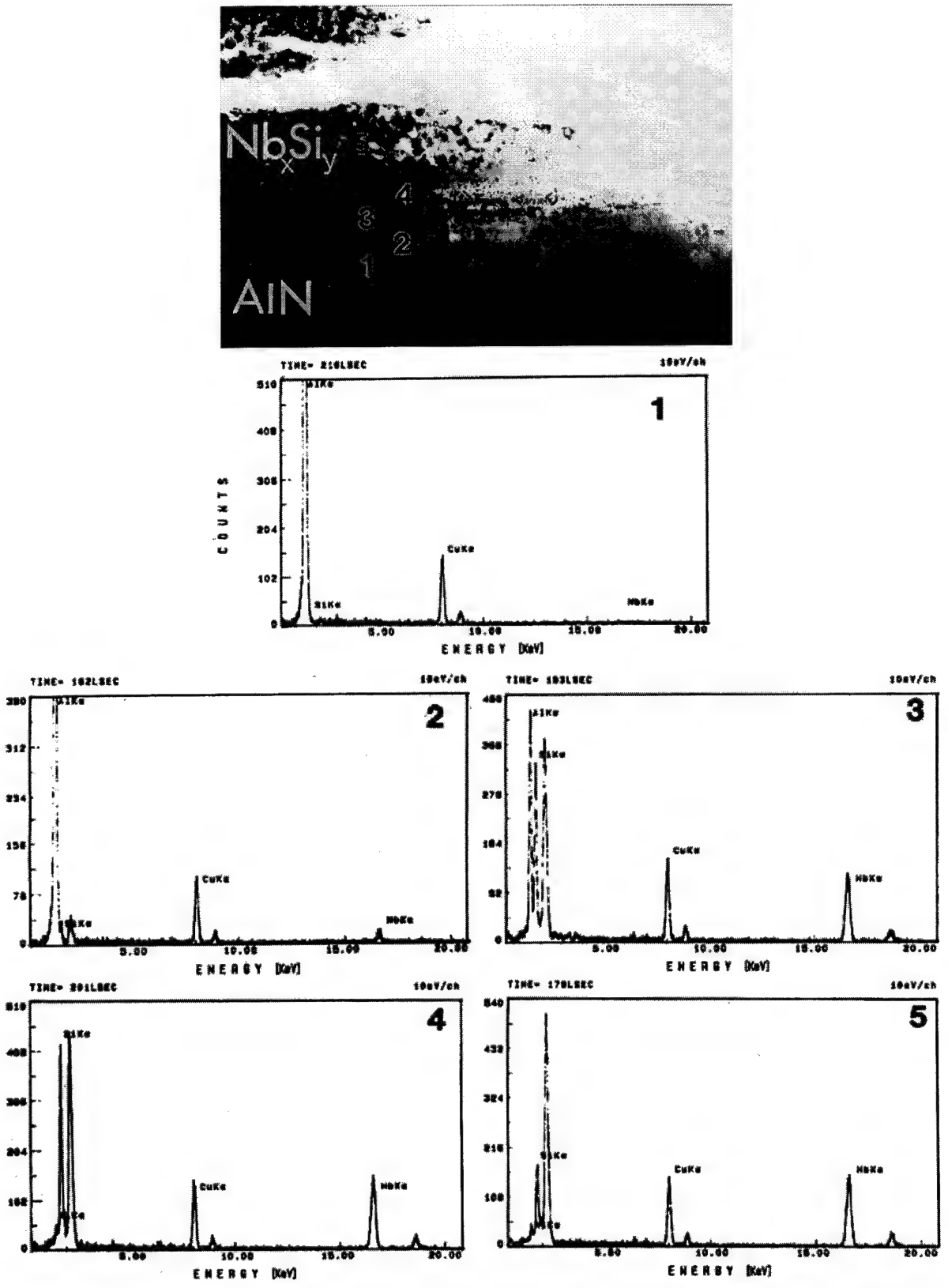

Figure 15. BF image of the Nb_xSi_y-AlN interfacial region with the positions of the spots indicated from which the EDS spectra were recorded and marked 1 through 5.

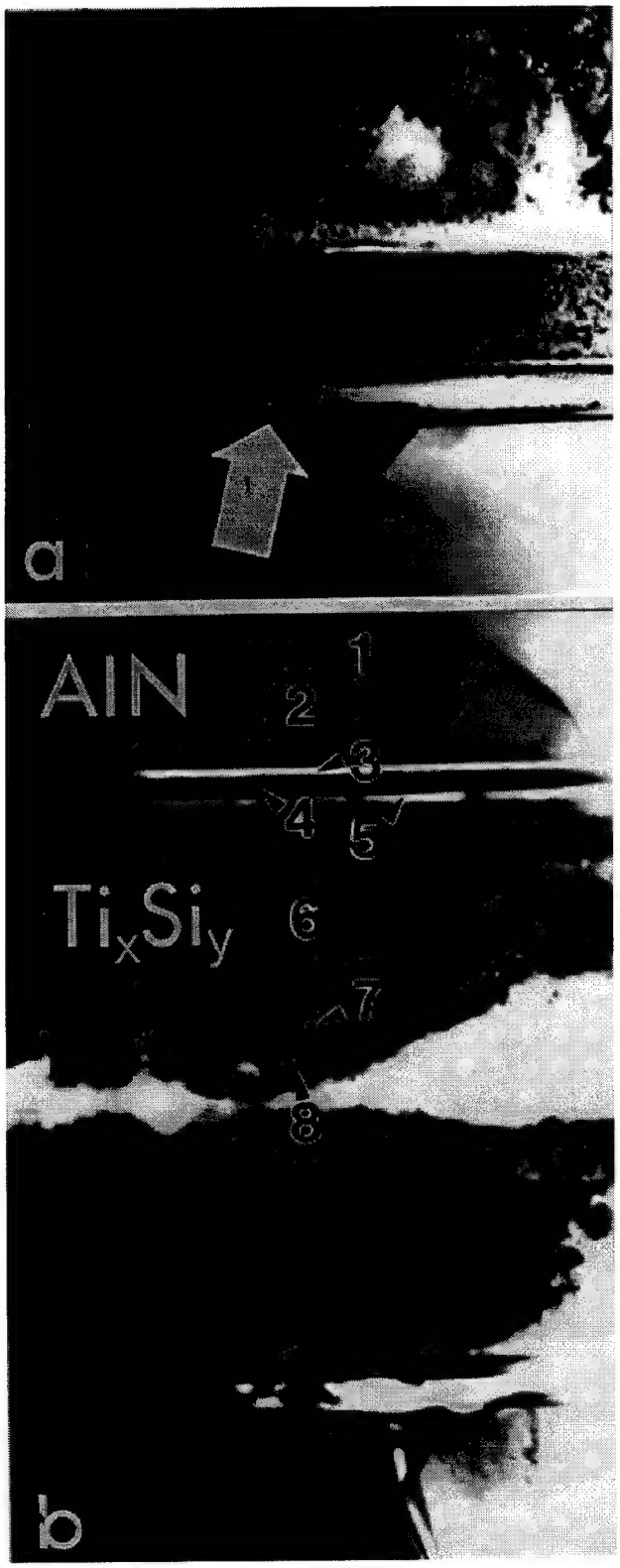

Figure 16. BF images of the region between the AlN substrate and the titanium silicide at 900°C. (a) Low magnification and (b) High magnification. The EDS spectra correspond to the compositions of the regions identified as 1 through 8 in (b). (Continued)

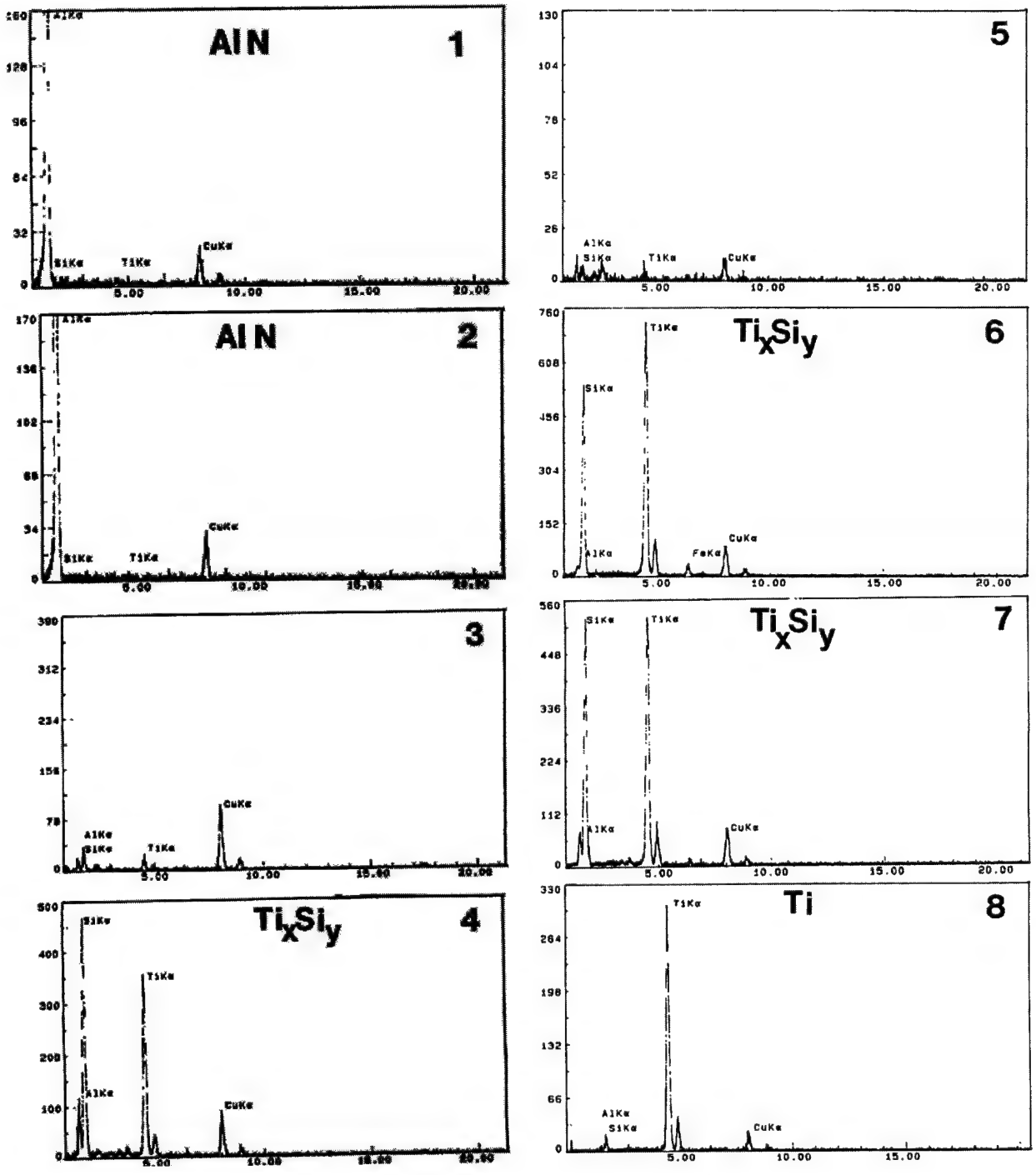

Figure 16. BF images of the region between the AlN substrate and the titanium silicide at 900°C. (a) Low magnification and (b) High magnification. The EDS spectra correspond to the compositions of the regions identified as 1 through 8 in (b). (Concluded)

Consequently, the regions between the titanium and the AlN correspond to various intermetallic compounds between Ti and Si (and possibly between Al and Ti also as titanium aluminides as well as ternary silicides among Al, Si, and Ti) depending on the elemental ratios as displayed in the corresponding EDS spectra. These results are not surprising from the fact that it has already been seen by equilibrium thermodynamic calculations that reactions between $TiSi_2$ and AlN were expected. The phases corresponding to the EDS spectra in Figure 16 (whose exact structures are not yet known) may potentially be related to both the equilibrium and metastable equilibrium phases, including the binary compounds between Si and Ti and Al and Ti as well as ternary system(s) among Al-Si-Ti.

WSi_2-deposited sample

Analyses of the interface between WSi_2 and AlN were also performed using the analytical TEM, nanodiffraction, and EDS analysis methods. Based on the thermodynamic stability calculations, it was expected that the interfaces would be more stable between AlN and WSi_2 than the previous two cases. Therefore, we performed analyses of the WSi_2-AlN samples that were heat treated both at 900°C and 1200°C.

Figures 17 and 18 correspond to the sample that was heat treated at 900°C. The BF image in Figure 17a was taken from the interface region between the AlN and WSi_2, and in the figures basically four different contrast regions are seen. These regions possibly correspond to four separate phases. Diffraction and EDS composition analyses were necessary to identify the phases at and near the interface. In the image, it is clearly seen that the AlN region is fairly featureless, except for some defects near the interface. The WSi_2 film incorporates polycrystalline elongated grains that are perpendicular to the interface plane (Figure 17). Nanodiffraction patterns taken from the silicide regions correspond to both WSi_2 and W_5Si_3 crystalline forms. To ensure the crystallinity of these regions and to assess how separate they are from the original phases, nanodiffraction analysis was performed. The diffraction patterns in Figures 17c through 17f correspond to the regions indicated by 1 through 4, in reverse order, in the BF image.

Both diffraction patterns 1 and 2 essentially correspond to the same type of zone axis and symmetry. Therefore, they correspond to the same phase, although pattern 2 came from a region next to the interface (also see Figure 18b). Clearly, in both the BF and DF images in Figure 18, the contrast in pattern 2 is significantly different than that in the matrix AlN region. The diffraction pattern taken from region 3 displays no elastic scattering, but it only gives the transmitted reflection; this is an indication that the thin strip of the phase at the interface has an amorphous structure. The diffraction pattern taken from region 4 displays several superimposed patterns presumably corresponding to several grains (WSi_2 and W_5Si_3) within the silicide film.

We also performed EDS analyses of these four regions to further assess their phase characteristics. The results are displayed in Figure 18, which also gives the BF image of the interface region from which the spectra were taken. Both of the spectra from 1 and 2 display only Al peaks, and the one corresponding to region 2 has significantly lower intensity. This is an indication that region 2 is significantly thin and, hence, has a smaller contributing volume for x-ray fluorescence. The EDS spectrum from the thin amorphous film displayed all of the peaks, i.e., Si-K_α, Al-K_α, W-L_α, and W-L_β as clearly indicated on the spectrum. Since the electron probe spilled over to both sides of this thin region, the corresponding elemental ratios do not necessarily reflect the true values of the phases. Finally, the EDS spectrum taken from the silicide displayed only Si and W peaks, corresponding to the two types of silicides that are present in this region.

From the EDS and nanodiffraction analyses, therefore, we conclude that region 2 corresponds to a transitory phase essentially incorporating only AlN and that there is thin amorphous film between this transitory region and the silicide film, whose stability, for now, is not yet clear.

The WSi2 AlN sample was also heat treated at 1200°C; the interface structure and properties were also evaluated using the cross-section samples as shown in Figures 19 and 20. The significance of the higher-temperature heat treatment turns out to be that there is no amorphous interfacial region in any of the

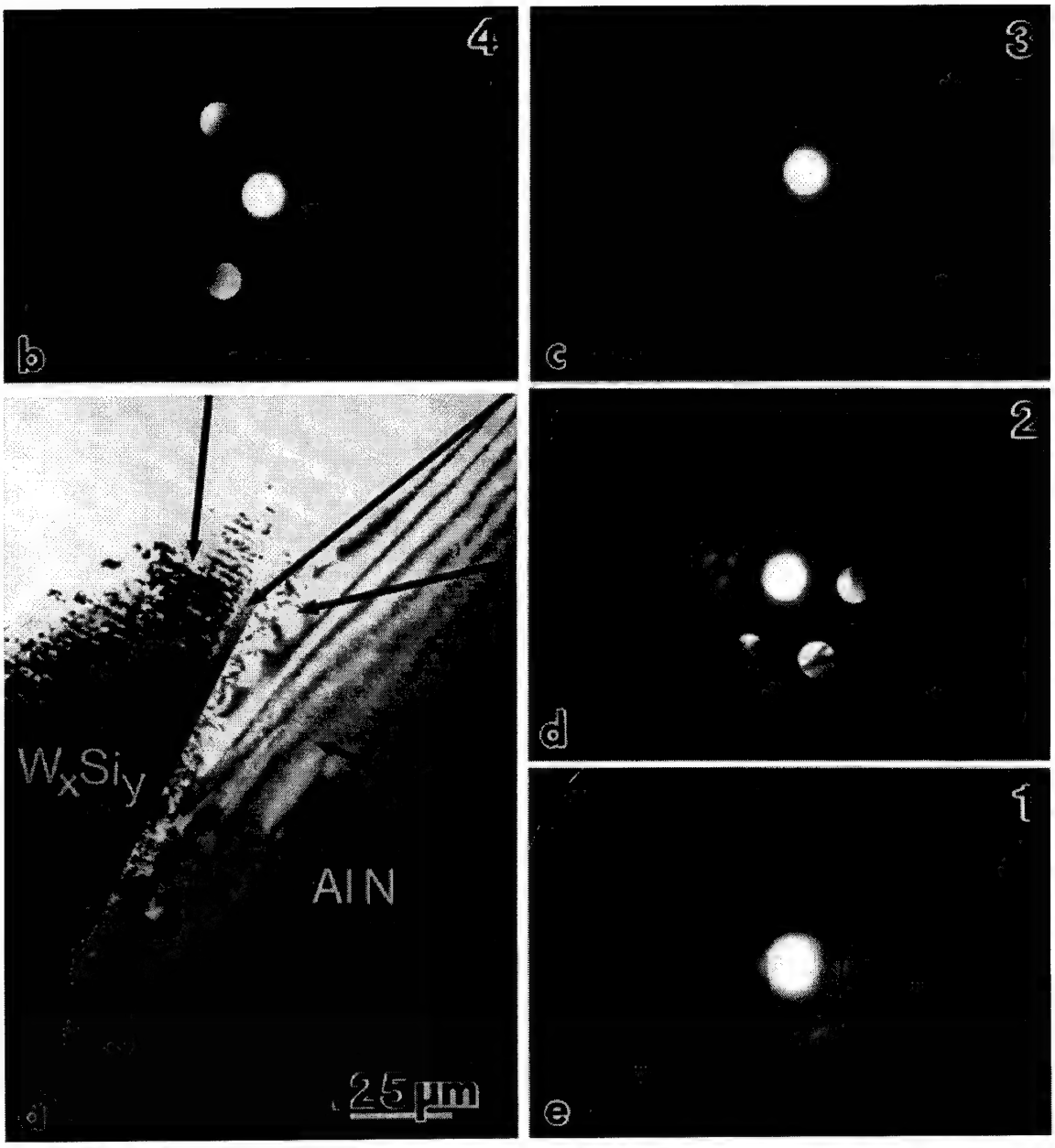

Figure 17. TEM analysis of the W_xSi_y-AlN sample after 900°C heat treatment showing the interface region. The arrows indicate the regions of the corresponding nanodiffraction patterns that were recorded.

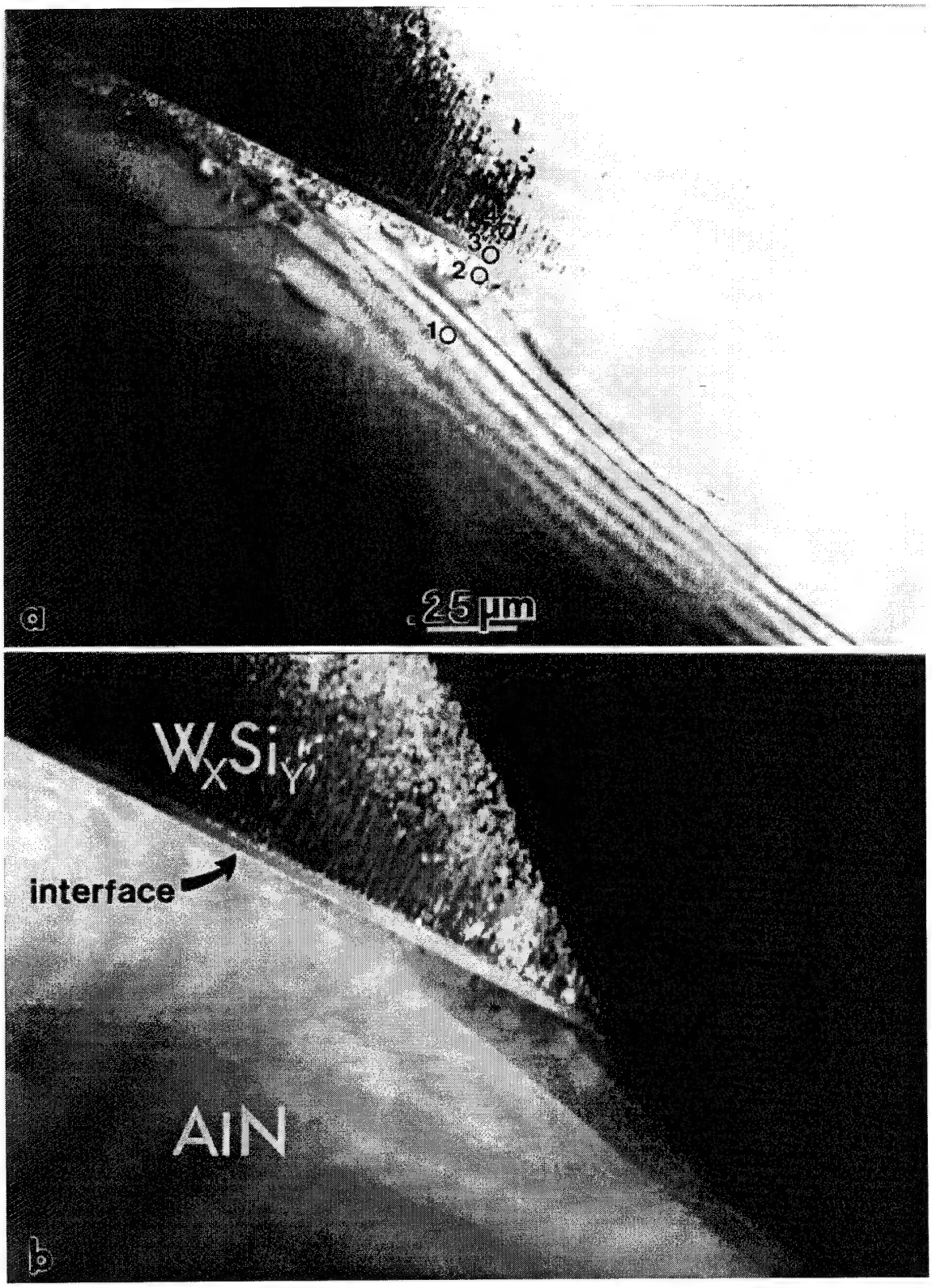

Figure 18. (a) TEM BF and (b) DF images from the W_xSi_y-AlN interface region at 900°C. EDS analysis results are shown in spectra (c) through (f), also numbered 1 through 4, respectively. (Continued)

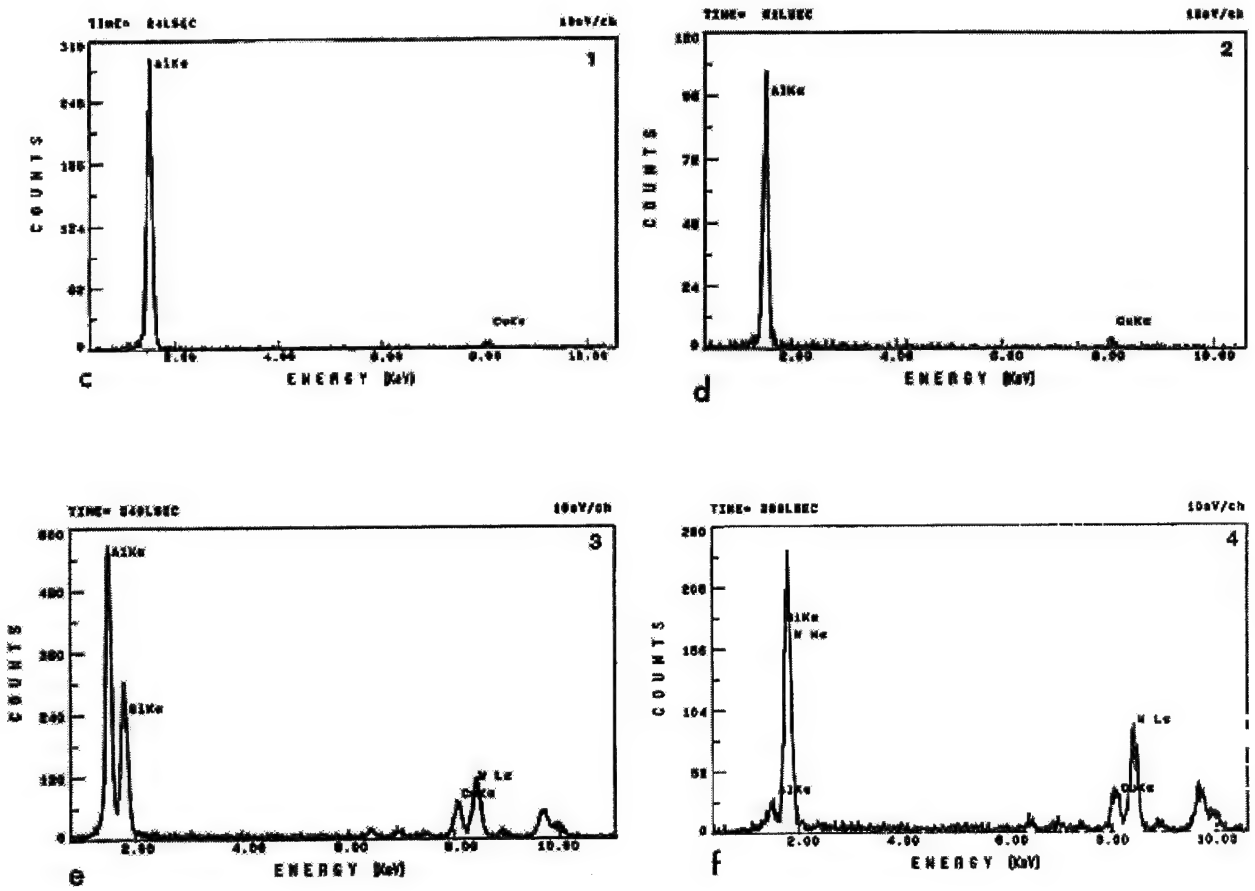

Figure 18. (a) TEM BF and (b) DF images from the W_xSi_y-AlN interface region at 900°C. EDS analysis results are shown in spectra (c) through (f), also numbered 1 through 4, respectively. (Concluded)

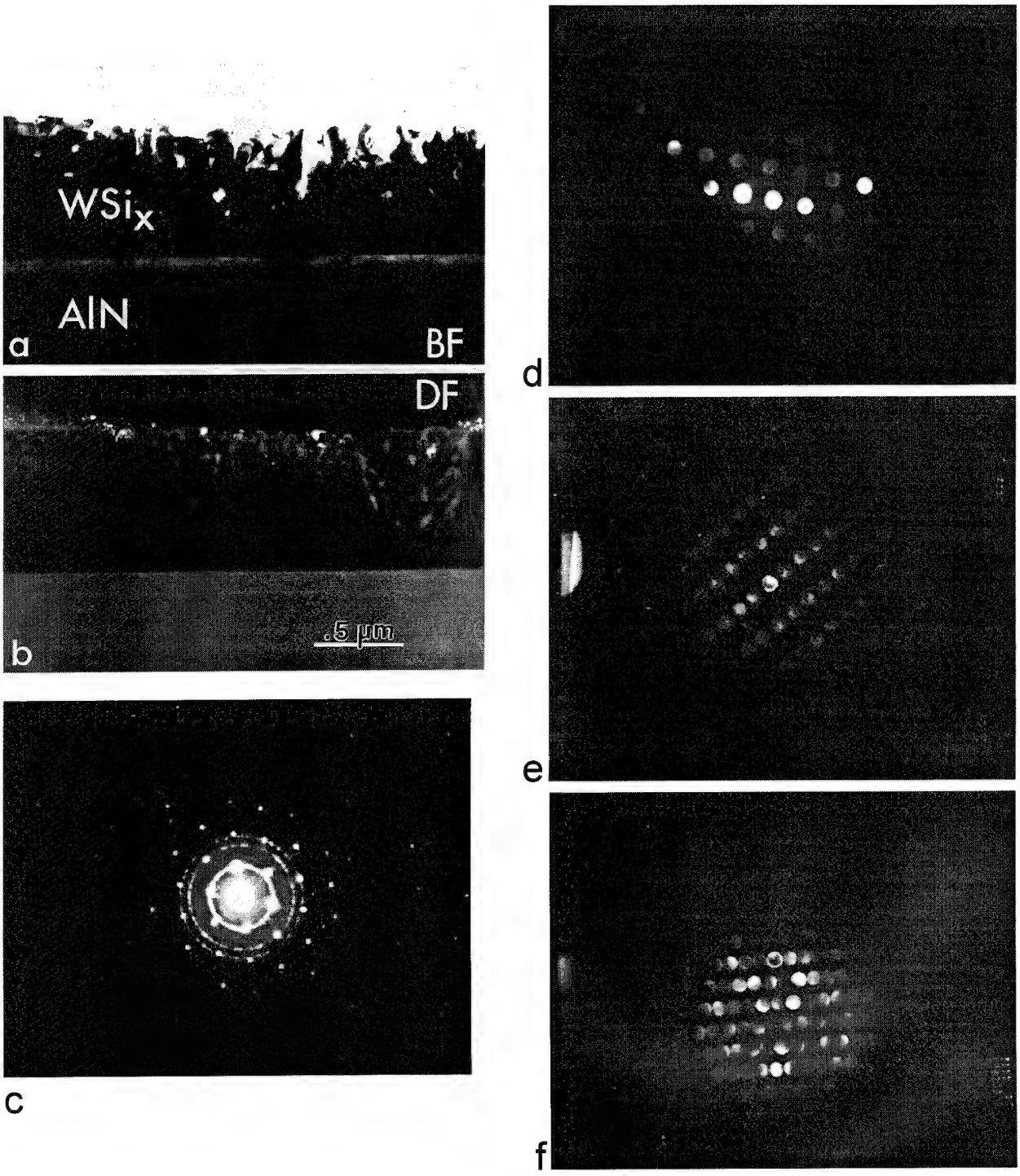

Figure 19. (a) BF and (b) DF images from the interface region of the 1200°C heat-treated WSi_2-AlN sample. Diffraction patterns (c) and (d) are from AlN and from the transition region. Nanodiffraction patterns (e) and (f) are from the individual nanograins within the silicide film.

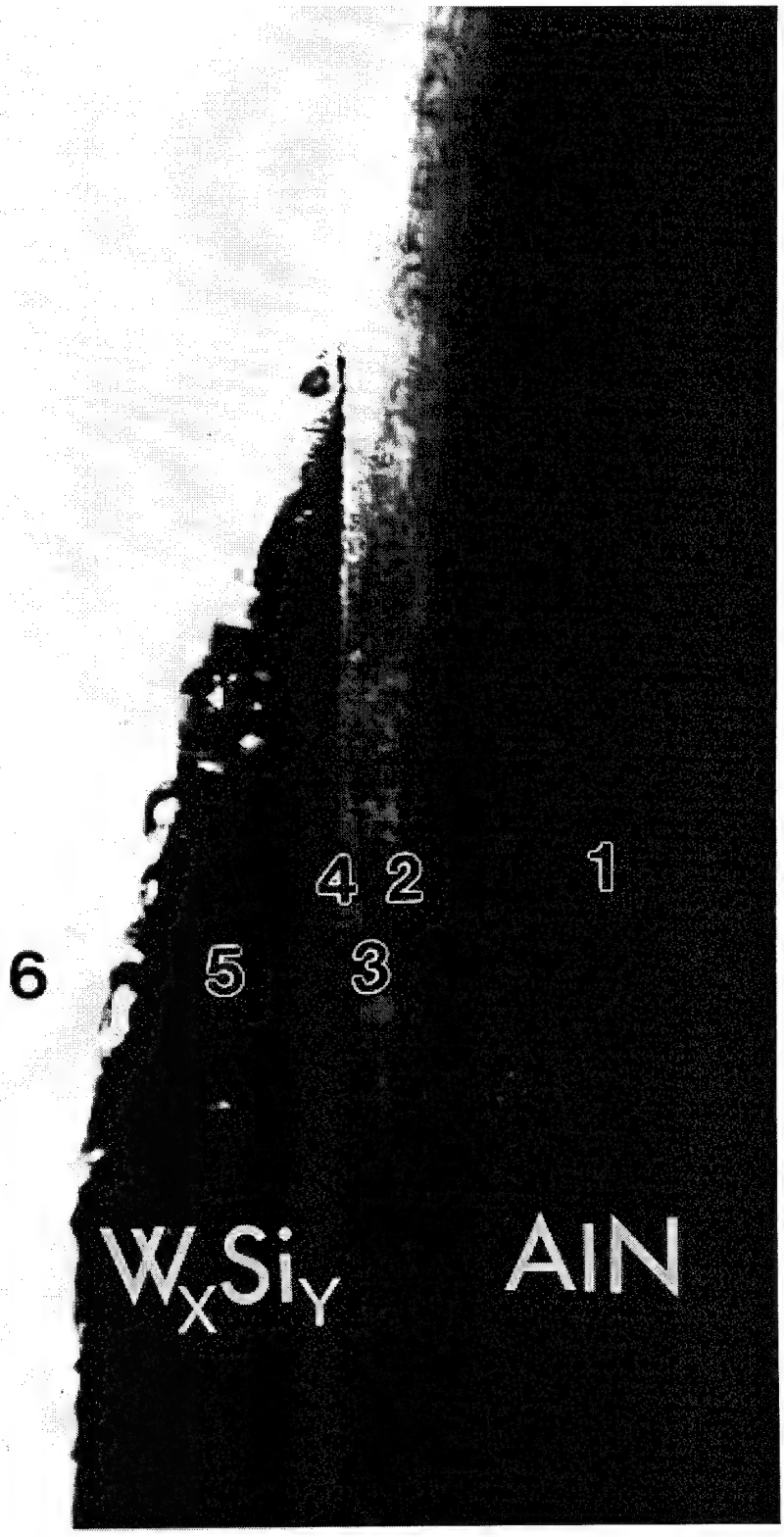

Figure 20. Elemental EDS analysis of 1200°C heat-treated WSi_2-AlN sample. The regions for analysis are indicated by 1 through 3 in the BF image. (Continued)

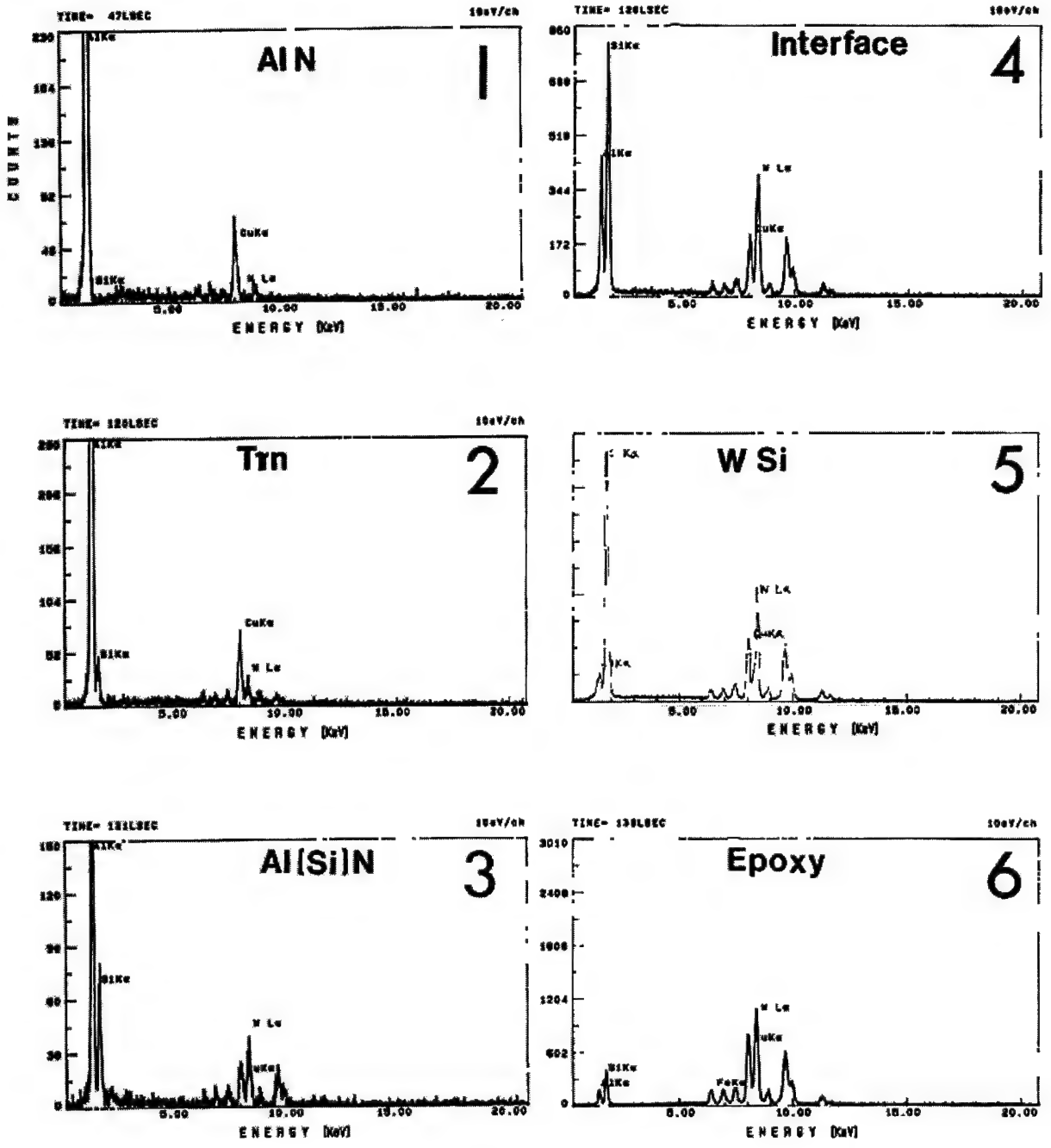

Figure 20. Elemental EDS analysis of 1200°C heat-treated WSi_2-AlN sample. The regions for analysis are indicated by 1 through 3 in the BF image. (Concluded)

samples examined. In addition, the transitory region seen in the 900°C sample (that had essentially the same structure as the AlN) now, after 1200°C heat treatment, displayed a much more defined layer with a slightly higher Si and W content, presumably due to dissolution of these elements in the AlN lattice. Figure 19 displays a BF/DF pair (a and b) that both show three distinct regions. Electron diffraction patterns taken from the interface transition region and from the AlN grain show the same pattern, which indicates that these two regions are isostructural. The nanodiffraction patterns taken from the silicide region indicate crystal structures corresponding to both the WSi_2 and W_5Si_3 phases. Another notable difference between this sample and the 900°C heat-treated sample is that the silicide grains, although only slightly grown, now have an equiaxial shape rather than the elongated shape that they displayed in the lower-temperature treatment.

Elemental analysis by EDS was performed in the three distinct regions as shown in Figure 20. The spectra identified as 1 through 3 correspond to the positions of the electron probe on the AlN, the transition region, and the W_xSi_y regions. While the Al peak is high in EDS spectrum 1, the Si peak starts appearing in spectrum 2. Again, in spectrum 3, only W and Si peaks are visible. We conclude from the EDS and diffraction analysis that the thin amorphous region in the 900°C heat-treated sample has disappeared upon the heat treatment at 1200°C and that the transition region seen at the lower temperature becomes more distinct in the higher-temperature sample with a partitioning of more silicon. The transition region essentially has the same crystal structure but with a certain amount of solubilized Si in it. In the W_xSi_y region, both crystalline forms of the silicide are present. Consequently, we conclude that W_xSi_y deposition after the 1200°C heat treatment provided an interface that is both structurally stable and has a good combination of physical properties as a candidate metallization.

6.2.2. Preparation and Characterization of WSi_2-SiC Sample

During package assembly, the IC chip is bonded (die attach) to the substrate using hard solders (Au-Si eutectic), brazes (Cu-Ag), epoxies, or glasses. For high-temperature applications, the choice is limited to high-end hard solders and brazes. Both of these operations require that the back side of the IC chip be metallized before bonding. Therefore, we have investigated $TiSi_2$, $NbSi_2$, and WSi_2 for SiC IC back-side metallization and have chosen WSi_2. The reasons for choosing WSi_2 are as follows:

- Chemical calculations showed that only WSi_2 is chemically compatible with SiC. Both $TiSi_2$ and $NbSi_2$ reacted with SiC, as shown in Figure 21.
- The AlN substrate also has WSi_2 metallization. This simplifies the die attach process, since both the substrate and the back side of the IC chip have the same metallization.
- Silicides, in general, have a great potential for IC device metallization such as gates, interconnects, Schottky barriers, and ohmic contacts for high-temperature applications. Therefore, establishing the chemical compatibility between SiC and silicide metallization will also establish the feasibility of silicides for SiC IC device metallization.

W_xSi_y films were deposited onto the SiC wafer, and its structure, stability, and chemical compatibility with SiC were examined.

Film deposition was done with RF sputtering from a WSi_2 target. The substrate temperature was kept at 400°C during the deposition process, which was carried out in an Ar environment. The as-deposited silicide was amorphous, which is similar to the case of silicide deposition on AlN. Therefore, in order to crystallize the silicide and evaluate its structural integrity, phase, and interface stability, we first heat treated the sample at 900°C for 1 hour in an Ar atmosphere. Similar to the preparation of AlN-silicide samples, the SiC-silicide sample was prepared for electron transparency using the cross-section sample preparation technique, and the sample was analyzed in terms of its structure, crystallinity, and elemental composition with an analytical TEM. The results are shown in Figures 22 and 23.

Figure 22, from the interface region, displays clearly that there are at least three separate regions with smooth boundaries between them. One of the most significant results from this image is that there

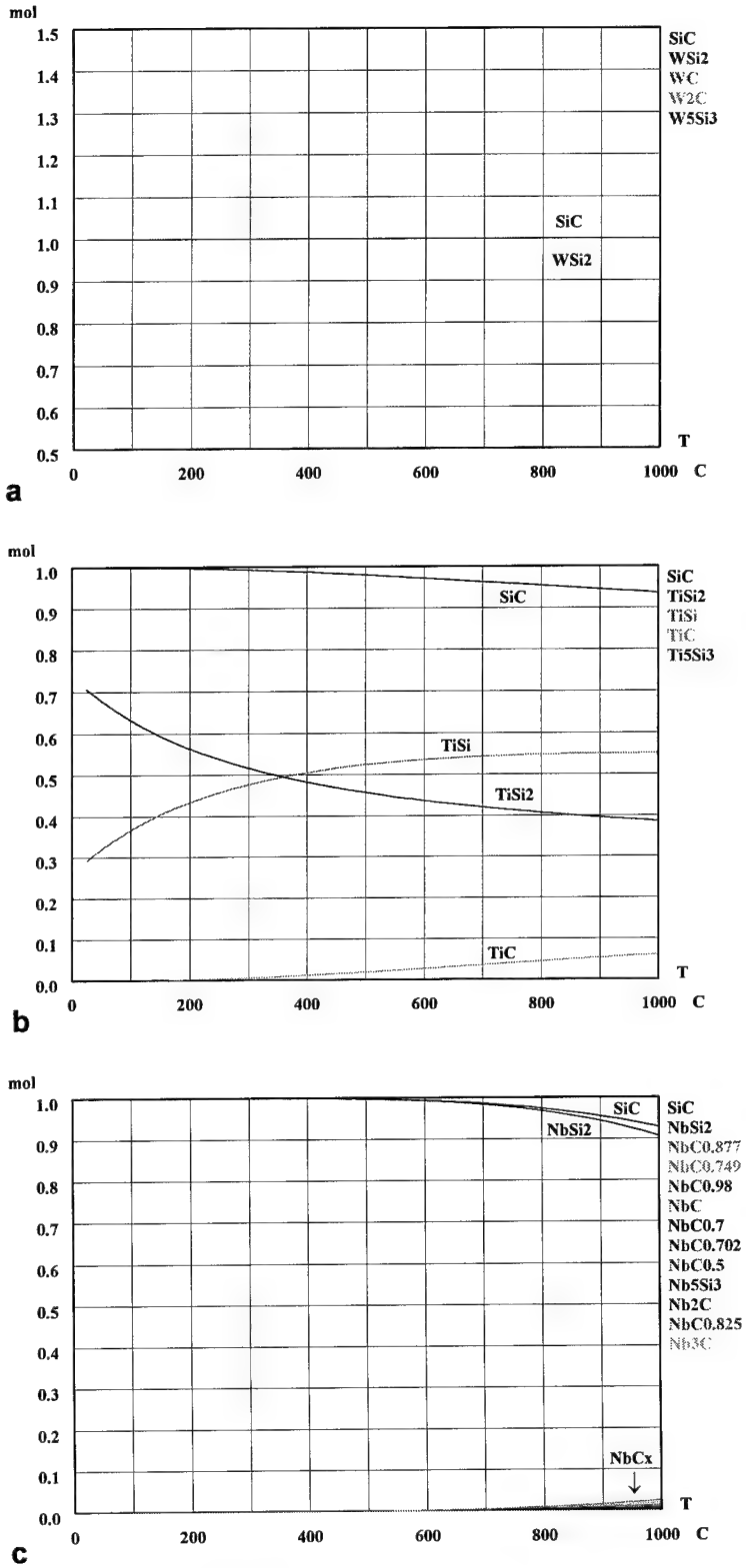

Figure 21. Graphical representation of chemical equilibrium calculations in (a) $SiC-WSi_2$, (b) $SiC-TiSi_2$, and (c) $SiC-NbSi_2$ systems.

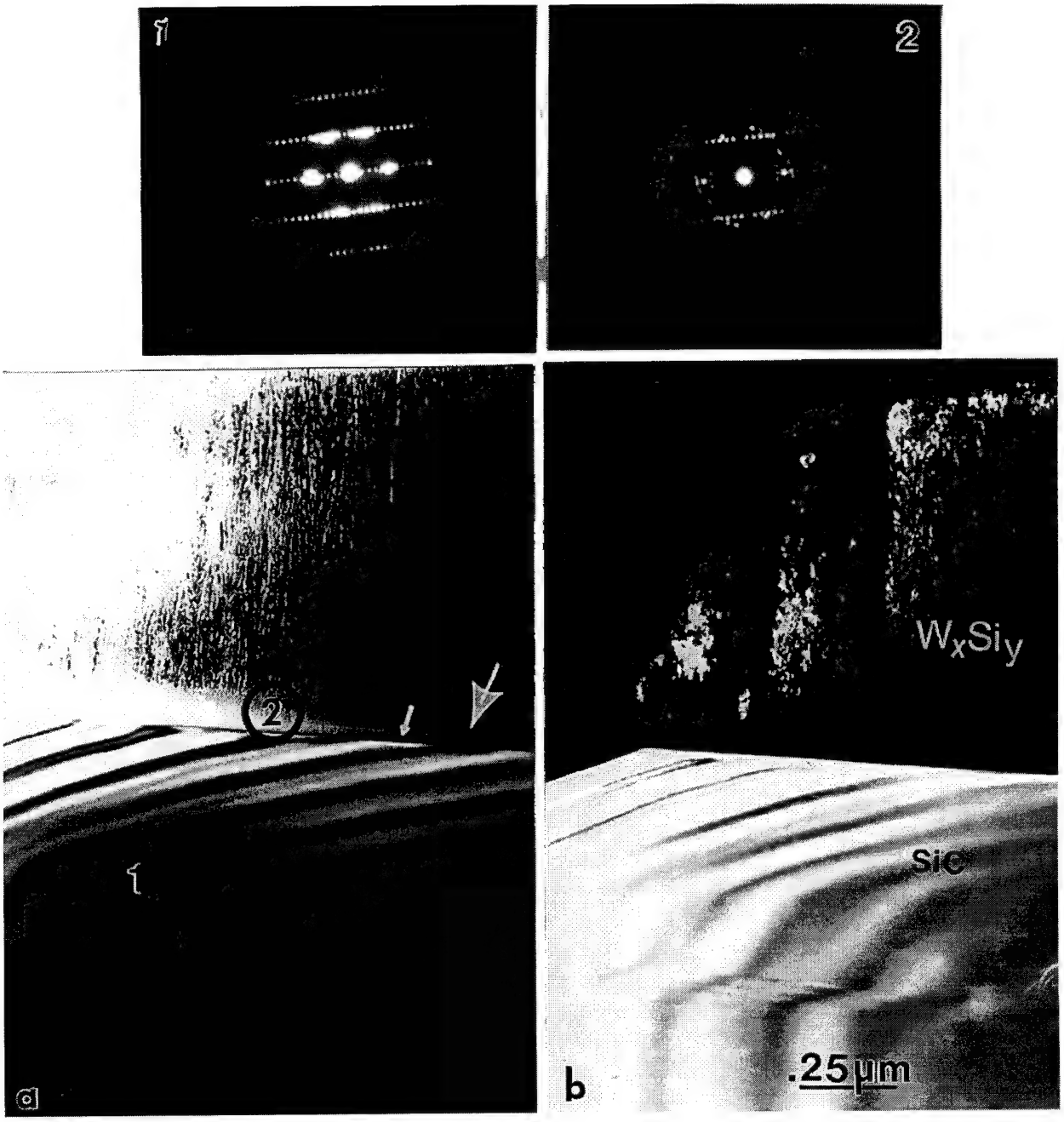

Figure 22. TEM analysis of the interface region between SiC and W_xSi_y. (a) and (b) are BF and DF images; the SAD patterns from the bulk SiC (number 1) and interface region (number 2) are also shown. The SAD pattern from the bulk SiC phase shows a repetitious 6 spot, a characteristic of the 6H structure.

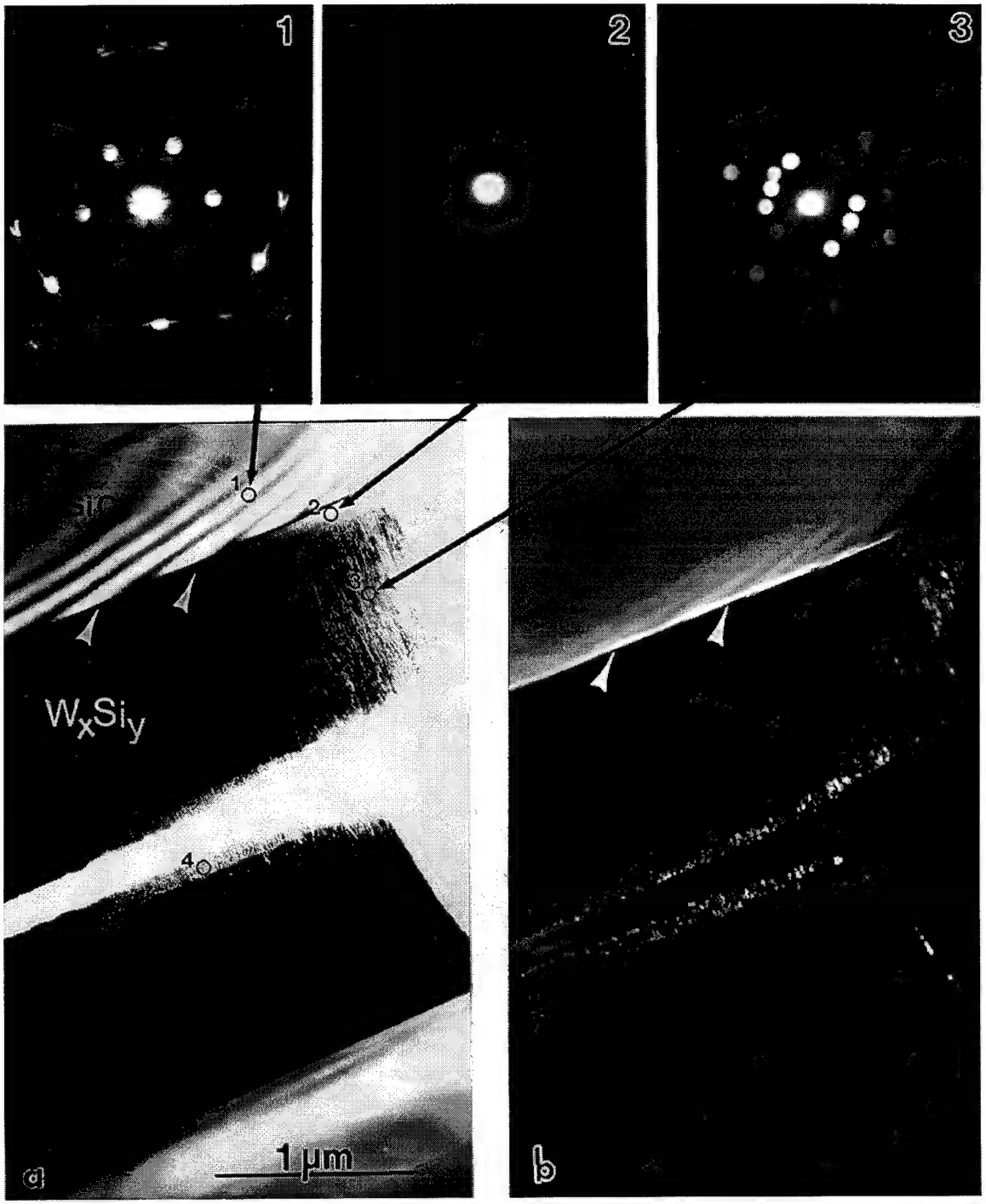

Figure 23. (a) BF and (b) DF image pair of the interface region with four separate layers (numbered 1 through 4) and the EDS spectra (c) through (f) recorded from these layers. (Continued)

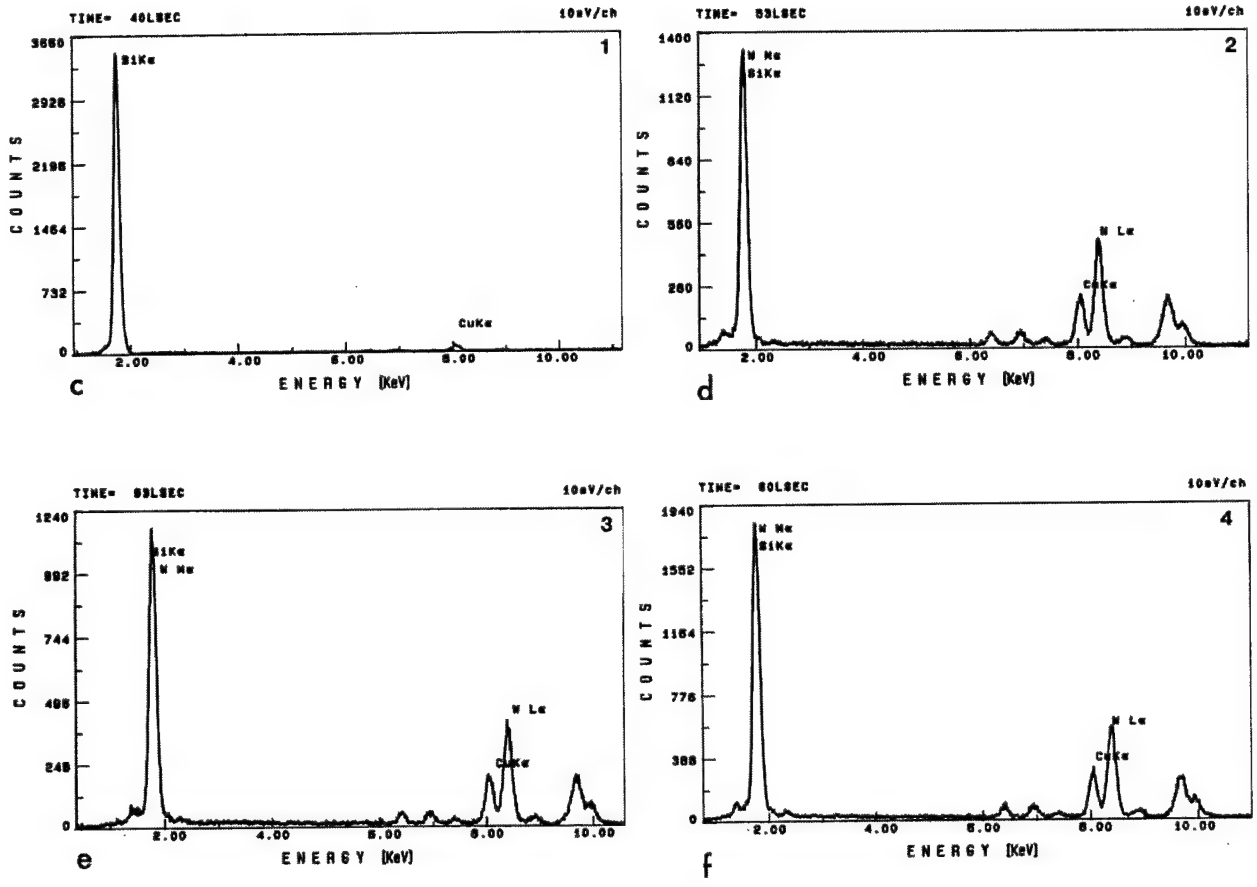

Figure 23. (a) BF and (b) DF image pair of the interface region with four separate layers (numbered 1 through 4) and the EDS spectra (c) through (f) recorded from these layers. (Concluded)

appears to be no interfacial reaction (as predicted by chemical equilibrium calculations) between the silicide and the SiC that results in rough interfaces with undesirable extraneous reaction products. Four regions are identified: the SiC, a thin layer between the silicide and the SiC, the silicide itself, and a thin layer on top of the silicide, marked by the number 4 in Figure 23a. It is already clear from the BF/DF images that silicide at this temperature has crystallized (in fact, XRD results indicate both WSi_2 and W_5Si_3 phases present at this condition). There is also a transition region between the SiC and the thin amorphous layer, as seen in Figure 22 and marked by the number 2. To confirm this conclusion, nano-diffraction patterns were obtained from the interfacial region using a probe about 200 Å in size. The results are displayed in Figure 23 (numbers 1 through 3). Both of the patterns shown in Figure 22, numbers 1 and 2, display a spot pattern indicating not only the crystallinity of SiC, but also that both are in the same zone axis orientation. As shown in the SAD pattern (Figure 22, numbers 1 and 2) the SiC belongs to the 6H crystal structure. The nanodiffraction pattern from the thin region on the W_xSi_y side displays diffuse scattering without any elastic reflection; this is an indication that this 500-Å thin film is amorphous (Figure 23, number 2). The last diffraction pattern taken from the elongated grains (Figure 23, number 3) on the W_xSi_y side displays multidiffraction patterns, indicating the poly-crystallinity of this region incorporating both forms of the silicide.

An elemental compositional analysis of the interface region was also done by energy-dispersive x-ray spectroscopy as shown in Figure 23. The region of interest is given in the BF image in Figure 23a, which displays the four layers of interest. The EDS spectra (Figures 23c through 23f) were taken from these four layers as shown by the numbered circles. Both regions 1 and 2 display only Si-K_α peaks (and not C-K_α since the energy for this peak, 382 eV, is too weak to be recorded by EDS). This result indicates that these regions are purely SiC. The amorphous region gives an EDS spectrum containing both the Si-K_α and W- L_α and W-L_β peaks. It is not yet clear whether this is a result of a chemical interaction between the SiC and silicide or this is a region of the silicide that has not yet fully crystallized upon the 900°C heat treatment. This issue will certainly be resolved by applying the higher-temperature heat treatment, as was done in the case of the W_xSi_y-AlN sample (in fact, as discussed, this amorphous region disappeared and there was a smooth interface between the AlN and W_xSi_y with a transition phase that was essentially all AlN). Finally, the EDS spectra shown in Figures 23e and 23f display a profile similar that in Figure 23d containing both Si and W peaks. The ratio of Si to W indicates that there are both WSi_2 and W_5Si_3 phases present in the crystalline region, again confirming the electron and x-ray diffraction results.

Atomic Force Microscopy Investigation of Domain Formation

The as-sputtered samples as well as the heat-treated samples were investigated both with atomic force microscopy (AFM) and transmission electron microscopy. The TEM results were described in detail in the preceding sections. Here we discuss the domain formation within a W_xSi_y sputtered sample on SiC. Figures 24a and 24b show images from as-sputtered and 1000°C heat-treated samples, respectively, using a large scan (40 μm x 40 μm) by a Park Scientific-CP AFM in air in the noncontact mode. Both of the images display regions of the sample in the plan view with a contrast that resembles domain formation. The size of the domains in both cases is about 5 to 10 μm. The only apparent difference between the two samples is the presence of pores in the as-sputtered samples (dark regions, indicated by arrows). These are annealed out in the heat-treated sample in Figure 24b, and the surface of the sample is smoother. Since in the AFM images the contrast arises from the height differences on the surface, the presence of domains indicates a certain degree of preferential growth of the W_xSi_y film on the substrate. However, what is interesting is the fact that the domain size and shape remain stable upon the heat treatment. Of course, with the AFM it is not clear whether the silicide film is amorphous at each of these two conditions and, hence, requires analysis by TEM. As discussed, the as-deposited films display no crystalline structure as evidenced by the absence of diffraction peaks in the XRD patterns (Figure 11). Further analysis of the heat-treated sample prepared in the cross-sectional configuration reveals the structure of the W_xSi_y in detail. Figure 24c and 24d are BF and DF images from the interface region between the silicide and the substrate. In the BF image (Figure 24c), there are columnar regions perpendicular to the interface. The DF image, recorded at a higher magnification, displays a contrast arising from the presence of elongated grains corresponding to these columnar regions. The individual silicide grains therefore appear to be about a few 100 Å and as long as several 100 nm extending across the thickness of the film. A more careful examination of this image reveals that the columnar grains are in fact in the form of bundles, the lateral size of which is about 5 to 10 μm. This result indicates that the bundles probably correspond to the domains that were seen in the AFM images. Regardless of the domain (or bundle) formation, the silicide film (with a thickness of about 1 μm) after heat treatment appears to be relatively uniform in structure consisting of the columnar grains with a smooth top surface.

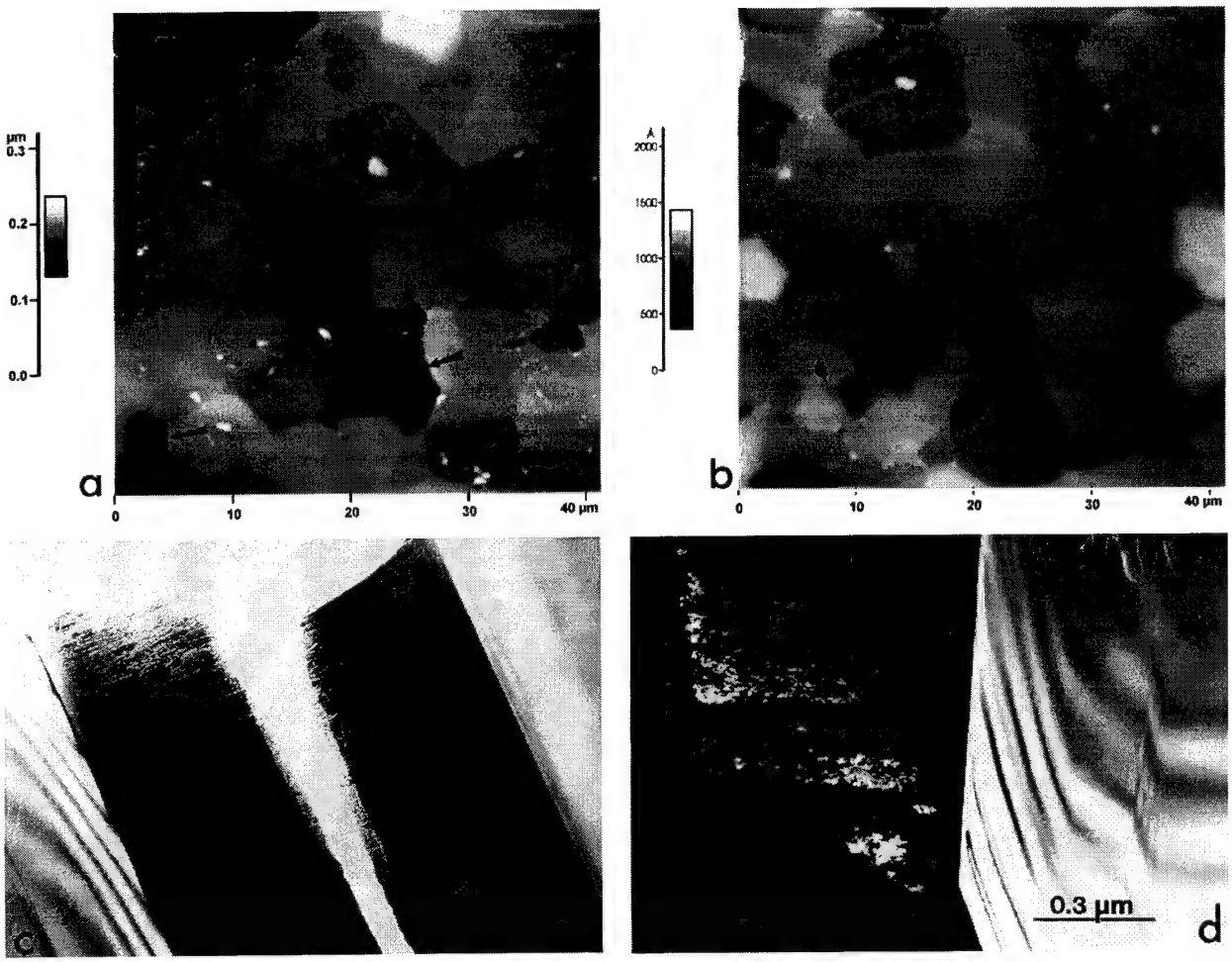

Figure 24. AFM images (a) before and (b) after 900°C heat treatment of W_xSi_y deposited on SiC revealing plan view microstructure; (c) TEM BF and (d) DF images showing the columnar grains of silicide across the deposited film.

7. PHASE I CONCLUSIONS

- In diffusion couple experiments, tungsten and niobium silicides appear to diffuse into the YAG phase present in aluminum nitride substrates, while titanium silicides do not diffuse into YAG. These behaviors need further investigation for a complete understanding.
- Tungsten, titanium, and niobium silicides RF sputtered from WSi_2, $TiSi_2$, and $NbSi_2$ targets have W_xSi_y, Ti_xSi_y, and Nb_xSi_y multiple stoichiometry and amorphous structures.
- Upon annealing, amorphous structures crystallize into mixtures of disilicides and polysilicides, i.e., WSi_2+W_2Si_5. Disilicide amounts must be maximized for high electrical conductivity if the silicides are to be used for circuit traces as well.
- The sheet resistivity of tungsten, titanium, and niobium silicides decreases with increasing annealing temperature. However, annealing temperature and time need to be optimized.
- The W_xSi_y-AlN interface, if free of any second phase, displays a transition region where silicon diffuses into AlN and forms a strong bond between the silicide and the AlN substrate. Therefore, the interface is expected to survive temperature excursions during assembly and operation.
- The Ti_xSi_y-AlN interface displays multiple amorphous and crystalline transition phases.
- The Nb_xSi_y-AlN interface also displays a reaction layer with multisilicide compositions.
- Refractory metal silicides, in particular tungsten silicides, appear to be promising for AlN metallization for use at 600°C and above.
- The SiC-W_xSi_y interface is fairly smooth and clean. It contains a transition region with SiC structure and a thin amorphous silicide layer between the SiC wafer and the W_xSi_y crystalline layer.
- Tungsten silicide is a potential back-side metallization for SiC IC chips.

8. SUGGESTIONS FOR FUTURE WORK

- Two-target sputtering to co-deposit tungsten and silicon to form stoichiometric tungsten disilicide on an aluminum nitride substrate and on the back side of silicon carbide wafers should be investigated to decrease the sheet resistivity.
- A detailed survey should be performed to identify candidate materials for die attach, wire bonding, lid sealing, and brazing.
- Plating of tungsten disilicide films should be investigated. A metal compatible with both tungsten disilicide and die attach and wire bonding materials to form a bond pad/diffusion barrier for die attach and wire bonding should be identified.
- Die attach, wire bonding, and brazing should be performed, and interfaces should be examined with advanced electron microscopy to ascertain their integrity.
- Adhesion between the tungsten disilicide, the aluminum nitride substrate, and the silicon carbide die; between the silicon carbide die and the aluminum nitride substrate; and between the wire and the bond pad should be measured before and after thermal cycling. Interfaces for mechanical integrity should be examined.

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ATTACHMENT
ALUMINUM NITRIDE PACKAGE FOR HIGH-TEMPERATURE ELECTRONICS

ALUMINUM NITRIDE PACKAGE FOR HIGH-TEMPERATURE ELECTRONICS

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ABSTRACT

Silicon carbide integrated circuit (IC) devices are being developed for use at temperatures over 600°C in military and civilian applications. Unfortunately, current packaging technology cannot handle these high temperatures. The package required for SiC chips is not readily available. Off-the-shelf packages lack thermal conductivity, thermal expansion coefficient match to the chip, and stable metallization. Aluminum nitride emerges as a candidate substrate and packaging material due to its high thermal conductivity, chemical stability, and thermomechanical compatibility with SiC. However, the current metallization technology cannot meet the performance requirements imposed by high temperatures. The present work presents an effort to develop a metallization system for AlN that will survive continuous operation at 600°C and above.

INTRODUCTION

There is a need for electronics that can operate at high temperatures. Applications that could use high-temperature electronics include well logging [1], aircraft and automobile engine control [2, 3], space exploration [4], nuclear reactors, and combustion sensors [5]. Silicon carbide integrated circuit (SiC IC) devices have been developed for use at temperatures up to 600°C in these applications. The ICs must be packaged to be protected from the harsh operating environment and to be integrated into the system they are part of. However, the required package for SiC ICs is not readily available. Off-the-shelf packages lack thermal conductivity, thermal expansion coefficient (CTE) match to the silicon carbide, and stable metallization at high temperatures.

Materials issues for high-temperature electronic packages include the following:

- Thermal conductivity
- Thermomechanical compatibility
- Chemical compatibility
- Hermeticity
- Simplicity, size, and weight

PACKAGING MATERIALS

A survey of current packaging materials for high temperatures, including ceramics and glasses, suggests that aluminum nitride (AlN) provides high thermal conductivity (200 W/m-K) and a CTE (4.3×10^{-6} °C^{-1}) similar to that of SiC (3.7×10^{-6} °C^{-1}), as shown in Table 1.

BeO is not considered as a viable candidate due to its toxicity and health hazards. Glass and glass ceramics suffer from low thermal conductivity and weak mechanical properties, while SiC suffers from low dielectric strength, high dielectric constant, and high dissipation factor, which can impact high-frequency or high-speed device operation. On the other hand, hot-pressed BN has a significant CTE mismatch with both Si and SiC in addition to its poor mechanical properties. Its chemical stability in oxidizing environments at high temperatures is also questionable. When compared to AlN, Al_2O_3 has a lower thermal conductivity and a higher dielectric constant. The temperature rise can cause Al_2O_3 to lose its already low thermal conductivity, while AlN still shows a thermal conductivity of over 100 W/m-K at 400°C as shown in Figure 1. Al_2O_3 has a CTE of 7.8×10^{-6} °C^{-1}, which significantly differs from that of SiC (3.7×10^{-6} °C^{-1}). The CTE

Table 1 - Material property comparison.

	Si	SiC	Al_2O_3	AlN	BeO	SiC	Borosilicate Glass	BN-hp
Density, g/cm^3	2.3	3.21	3.75	3.31	2.90	3.21	2.13	25
Hardness, GPa	11.5	24.0	19.0	12.0	12.0	24.0	-	2.5
Strength, MPa	250	450	350-400	350-400	200-250	450	70	53
Elastic modulus, GPa	130	470	397	320	345	420	195-265	43
Thermal conductivity, W/m·K	150	300	25	200	250	70	4.0	25
Thermal expansion coefficient, ppm/°C	3.5	3.7	7.2	4.1	8.0	3.7	3.25	0.3
Resistivity, ohm-cm	--	--	$>10^{14}$	$>10^{14}$	$>10^{14}$	1	10^{11}	10^{11}
Dielectric constant (@ 1 MHz)	11.0	42	9.4	8.9	7.0	42	4.6	4.1
Dissipation factor (@ 1 MHz)	0.09	0.05	0.0004	0.0005	0.0003	0.05	0.002	0.0045
Dielectric strength, kV/mm	--	--	15	15	10	0.7	--	--

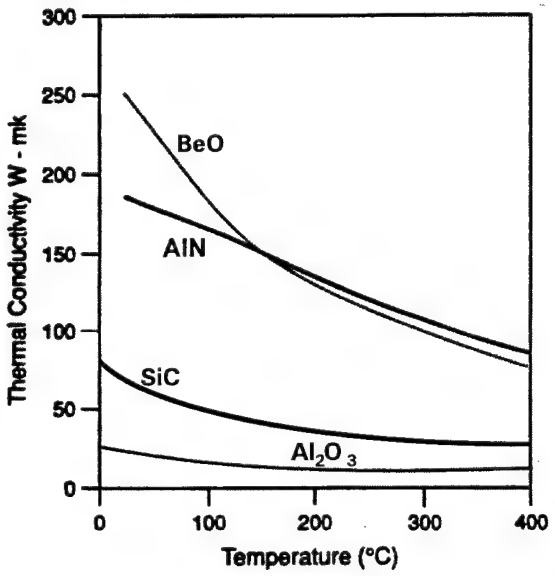


Figure 1 - Thermal conductivity of commercial AlN, SiC, BeO, and Al_2O_3 [6].

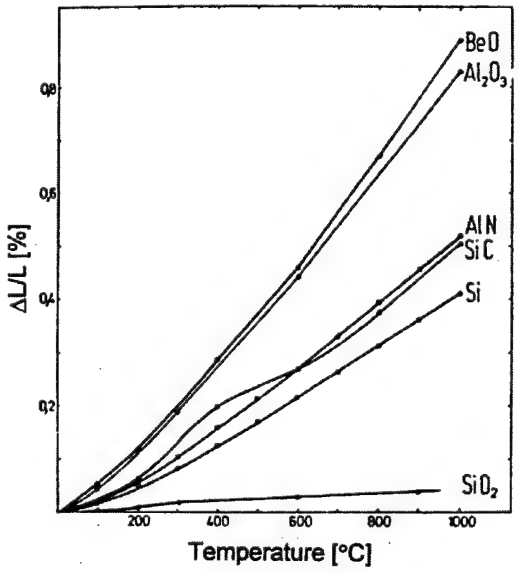


Figure 2 - Thermal expansion of AlN, Al_2O_3, and BeO in comparison to that of SiC and Si [7].

mismatch causes thermal residual stresses that then lead to device failures. This problem can be totally eliminated if one uses AlN, since its CTE is very close to that of SiC as illustrated in Figure 2.

As the temperature rises, the dielectric constant of oxide ceramics increases rapidly as shown in Table 2. However, because AlN is mostly covalent, the dielectric constant and dielectric loss rise little with increasing temperature as shown in Tables 2 and 3, respectively.

In summary, AlN appears to be an ideal candidate for high-temperature packaging applications over 600°C. Some of the important advantages of AlN include the following:

- A CTE that closely matches those of Si and SiC, which minimizes thermal stresses.
- High thermal conductivity, which decreases only slightly with increasing temperature.
- Good thermal shock resistance and environmental stability at high temperatures.
- Nontoxicity (unlike beryllia).
- High electrical resistivity.
- High mechanical strength.
- Chemical inertness at high temperatures.

Table 2 - Dielectric constants for various materials as a function of temperature.

Material	Kr 23°C	Kt/Kr 1000°C	Kt/Kr 1200°C	Kt/Kr 1400°C
Fused silica (high purity)	3.82	1.02	1.03	1.04
Spinel ($MgAl_2O_4$)	8.2-8.4	1.19	1.25	--
Boron nitride	4.2-4.5	1.05	1.07	1.09
Silicon nitride	7.5-8.8	1.08	1.11	1.16
Alumina	9.5-9.8	1.15	1.21	1.27
Beryllia	6.6-6.8	1.16	1.24	1.32
Aluminum nitride	8.3-8.5	1.10	1.13	---

Table 3 - Dielectric loss (tangent δ) of AlN as a function of temperature.

Temperature (°C)	Tan δ
23	0.0011
250	0.0017
523	0.0023
805	0.0050
893	0.0120
920	0.0190
950	0.022
1000	0.032

METALLIZATION

Before the potential of AlN for high-temperature electronic packaging is realized, the metallization issue must be resolved. Currently, no metallization is available that is suitable for AlN in high-temperature applications. Metallization problems at high temperatures include the following:

- The reactivity of metallization with its surroundings increases.
- The resistivity of metallization increases.
- An increase of electron migration occurs due to enhanced diffusion
- The difference between the CTE of the metallization and that of the substrate increases with increasing temperature. CTE mismatch causes thermal stresses that lead to failures.

An ideal high-temperature metallization should have the following properties:

- High melting point over 600°C
- Low electrical resistivity
- Low-temperature coefficient of resistance
- Matching CTE with AlN
- High bond strength between metallization and AlN
- High thermal conductivity

In package construction, all materials used must have melting points well above 600°C. The materials must also have a hierarchy of melting temperatures that permits the desired sequence of assembly, i.e., die attachment then sealing and lid attachment. However, this hierarchy does not need to be rigid, because some attachment steps may involve only local or transient heating.

Metallic conductors are used in metallization and in interconnects in multi- and single-layer electronic packages. Traditional precious metals in hybrid circuit technology are replaced by other materials because of the requirement for high-temperature applications and because of the economics. As a rule of thumb, the melting temperature should be 1.5 times higher than the operating temperature to prevent any diffusion-related problems. These considerations eliminate some of the commonly used metals, such as silver (T_m = 961°C), as a candidate. The selection of a conductor requires careful consideration because of the many limitations imposed by the processing and by the operating conditions under which the devices operate.

The large CTEs of metals ($10 - 17\times10^{-6}$ °C^{-1}) can give rise to large thermal stresses, which can cause device failures. Refractory metals such as W, Mo, Ta, Zr, and Ti may be suggested. However, W and Mo do not adhere to AlN and require a protective coating to prevent oxidation. Ta, Zr, and Ti show some promise, as thermodynamic calculations suggest the formation of aluminides that can act as an interface between AlN and these metals.

Refractory metal silicides and borides represent the best performance/compromise mix for applications at 600°C and above. These may not be ideal solutions to the problem but represent rather the most promising approach. Some of the most promising candidates are refractory silicides and borides of tungsten, tantalum, titanium, and molybdenum, as shown in Table 4. Refractory silicides and borides have CTEs ($5 - 7\times10^{-6}$ °C^{-1}) that match both AlN and SiC, thus minimizing potential thermal residual stress problems. They also have low electrical resistivities: 6 microohm-cm for $CoSi_2$ and $TiSi_2$ and 12.5 microohm-cm for WSi_2 [8]. These materials can be deposited by conventional CVD techniques and patterned using conventional lithographic techniques on AlN.

Table 4 - Electrically conductive materials.

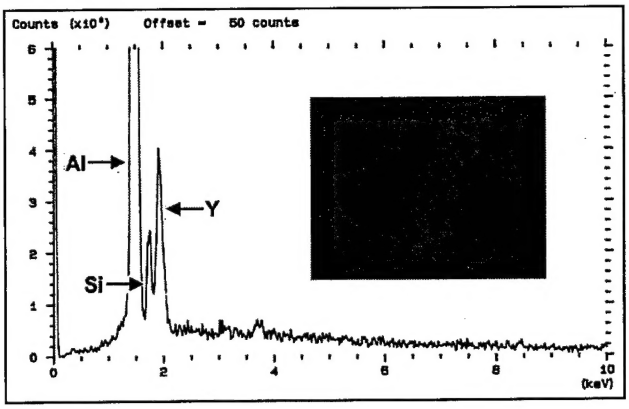
Material	Resistivity (μΩ-cm)	CTE ($\times 10^{-6}$ °C^{-1}) @ 27 °C
Cu	1.5	17
Au	2.0	14
Al	2.4	25
W	4.8	4.5
Mo	5.0	5.0
Ni	6.0	13
Co	6.2	12
Pd	9.8	8.5
Pt	10.6	9.0
Ta	12.2	6.5
Nb	12.5	7
Ti	42.0	8.5
$TiSi_2$	*≈ 6.0*	*7.5*
$CoSi_2$	*≈ 6.0*	*7.5*
$NbSi_2$	*6.3*	*7.0*
$TaSi_2$	*8.5*	*8.3*
$MoSi_2$	*22*	*5.1*
WSi_2	*12.5*	*8.3*
ZrB_2	*7*	*7.6*
TiB_2	*9.0*	*6.8*
NbB_2	*12*	*6.5*
ZrN	*13.6*	*7.0*
TiN	*21.7*	*6.6*
Diamond	$>10^9$	0.8

EXPERIMENTAL RESULTS AND DISCUSSION

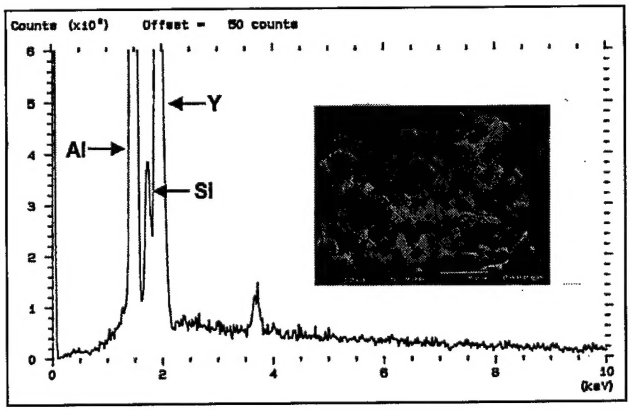
Even though we have investigated WSi_2, $TiSi_2$, and $NbSi_2$, here we will report only on WSi_2. The work on $TiSi_2$ and $NbSi_2$ will be reported in the future. AlN-WSi_2 diffusion couples were prepared and heat treated at 1200°C for 1 hour in a flowing argon atmosphere in a boron nitride crucible. AlN was sintered with yttria additive so that it contained a yttrium-aluminum garnet phase at triple grain boundaries.

For the diffusion couple experiments, an AlN substrate and a WSi_2 block were polished to a surface roughness of Ra=0.05 μm. They were mechanically coupled and placed in the crucible. After heat treatment, the AlN surface was examined under scanning electron microscopy (SEM). Figure 4 shows SEM photos of the AlN surface along with the energy dispersive x-ray spectrographs (EDSs) of the surface.

It is clear that WSi_2 reacts with AlN. The reaction appears to involve not only AlN, but also a garnet phase in the



(a)



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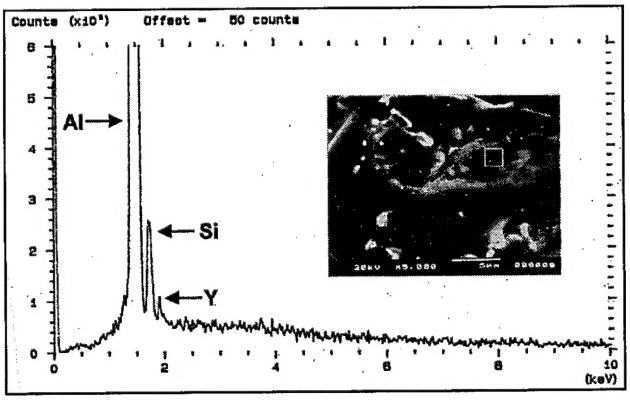

(c)

Figure 4 - Micrographs and EDSs of AlN surface after heat treatment (with increasing magnification).

AlN as evidenced by the presence of the yttrium peak in Figure 4. There is no W peak in Figure 4. This is because W-K_α peak emission occurs at 16 keV and cannot be excited with available voltages in our SEM. However, the presence of the silicon peak suggests that garnet also reacts with WSi_2.

A WSi_x film was deposited on the polished AlN substrate by the rf sputtering technique using a hot-pressed WSi_2 target. The deposited films were heat treated in argon at 900°C, 1000°C, and 1200°C for 1 hour. Sheet resistivities, measured by the four-point probe technique, are tabulated in Table 5.

Table 5 - Sheet resistivity of WSi_X films.

Condition	Sheet Resistivity (Ω/□)
As deposited	4.33
900°C	1.95
1000°C	1.33
1200°C	0.65

The values listed in Table 5 favorably compare to those of refractory metal (W or Mo) metallization. A detailed analysis of the structure of the thin WSi_X film and the interface region was performed by transmission electron microscopy (TEM). Figures 5a and 5b show bright field (BF) and dark field (DF) images, respectively. The WSi_X layer is quite uniform and is about 0.7 μm thick. To determine the crystal structure of WSi_X, micro-diffraction patterns were obtained from individual crystallites as shown in Figures 6a and 6b. The patterns indicate the presence of both WSi_2 and W_5Si_3, suggesting that WSi_X is a mixture of both WSi_2 and W_5Si_3.

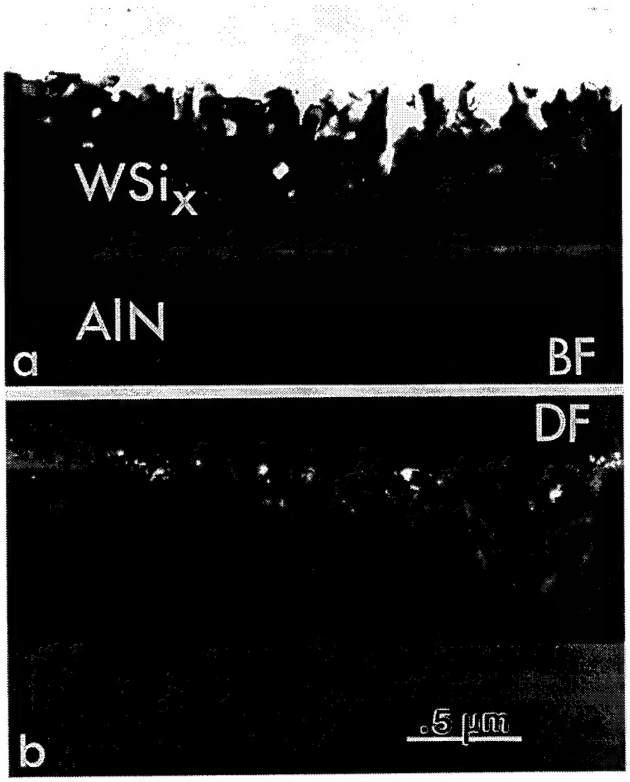

Figure 5 - TEM micrographs of AlN/WSi_x interface (a) Bright field image; (b) Dark field image.

The TEM observation of the AlN/WSi_x interface showed the presence of a transition region between AlN and WSi_x. Micro-diffraction patterns and electron spectroscopy indicated that the transition region is similar in crystallography and composition to AlN as shown in Figures 6c and 6d. It is possible that Al may be incorporated into WSi_x and/or Si may be incorporated into the AlN matrix. However, this hypothesis needs further study.

The absence of a secondary extraneous phase at the AlN/WSi_x interface indicates successful metallization. The existence of a transition region, having fundamentally the same characteristics as the AlN phase, is advantageous to the stability of the metal/substrate interface. Having a transition region similar in structure to that of AlN means that, even at 1200°C, the interface would be stable chemically and the transition region would have similar thermomechanical properties, eliminating thermomechanical incompatibility problems.

CONCLUSIONS

- Aluminum nitride is an excellent material for high-temperature (600°C and above) packaging of silicon carbide integrated circuit devices.
- A WSi_x film was sputtered and heat treated in argon. The sheet resistivity of WSi_x decreases with increasing annealing temperature.
- Transmission electron microscopy showed that tungsten disilicide adheres to aluminum nitride via possible silicon diffusion into the substrate. The aluminum nitride/tungsten disilicide interface is free of any second phase and is coherent. Therefore, it is expected to survive temperature excursions.
- The WSi_x phase appears to be a mixture of WSi_2 and W_5Si_3.
- Metal silicides appear to be promising for aluminum nitride metallization for use at 600°C and above.

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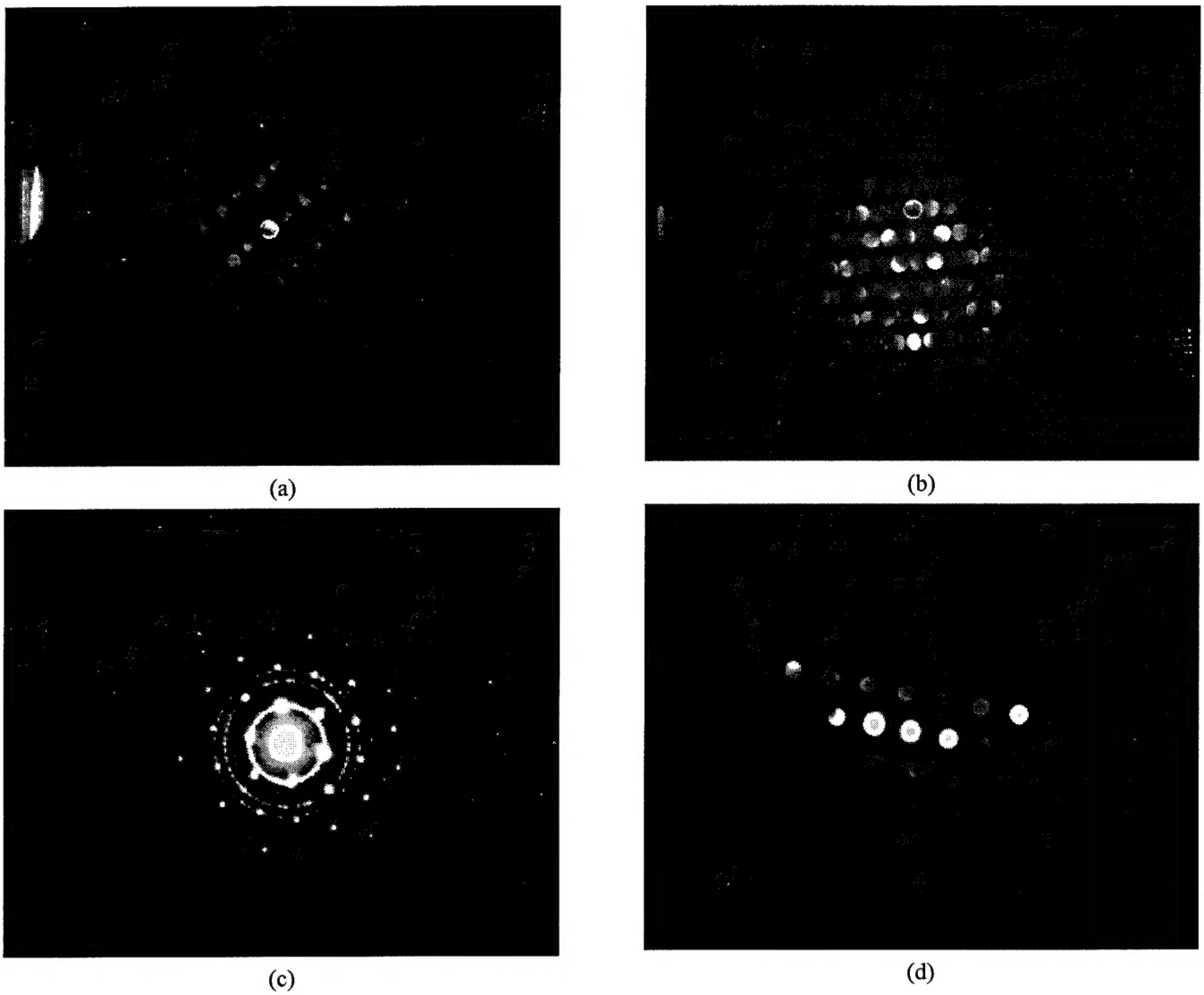

Figure 6 - Electron micro-diffraction patterns of (a) WSi_2, (b) W_5Si_3, (c) Interface, and (d) Transition region.

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